4) [20 points] Address Translation

Consider a system where the virtual memory page size is 2K (2048 bytes), and main memory consists of 4 page frames. Now consider a process which requires 8 pages of storage. At some point during its execution, the page table is as shown below:

Virtual page	Valid	Physical page
0	No	
1	Yes	0
2	Yes	1
3	No	
4	Yes	3
5	No	
6	No	
7	Yes	2

a) List the virtual address ranges for each virtual page.
b) List the virtual address ranges that will result in a page fault.
c) Give the main memory (physical) addresses for each of the following virtual addresses (all numbers decimal): (i) 2050, (ii) 4100, and (iii) 7000.
d) Compute an expression for optimal page size that minimizes memory use for the scheme.

7) [20 points] Page Replacement

Using the following reference string, calculate the number of page faults. Clearly mark each hit or miss in the table.

0 1 2 3 0 1 4 0 1 2 3 4

a) Frame Size = 3 (Replacement policy FIFO)

Ref String	0	1	2	3	0	1	4	0	1	2	3	4
Hit/Miss												

Page Faults : _____

b) Frame Size = 4 (Replacement policy FIFO)

Ref String	0	1	2	3	0	1	4	0	1	2	3	4
Hit/Miss												

Page Faults : _____

c) Frame Size = 4 (Replacement policy LRU)

Ref String	0	1	2	3	0	1	4	0	1	2	3	4
Hit/Miss												

Page Faults : _____

d) Compare the behavior part a, b and c. What is a stack algorithm? Is FIFO a stack algorithm? Why or Why not? Use the example above to explain.

8) [20 points] Demand Paging

Suppose that we have the following system characteristics:

System Characteristics	
Size of memory	16 bytes
Page Size	4 bytes per page
Memory Management Structure	Inverted Page Table
Replacement Policy	LRU, Global Replacement
Virtual Page Size	4 bytes per page
Virtual Address Space Size	32 bytes
Backing Store Size	12 blocks
Backing Store Block Size	4 bytes per block

And the following system snapshot

Main Memory

Address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents	O	T	O	N	G	F	U	N	-	-	-	-	A	D	*	F

Backing Store

Block	0	1	2	3	4	5	6	7	8	9	10
In Use?	T	T	T	T	T	T	T	T	T	T	T
Contents	THRE	AD*F	UNDO	RATE	*MON	OTON	ICCO	DEMA	ND*P	AGIN	GFUN

Process Table

Process ID	0	1	2
Process Size (Bytes)	10	14	16
Pages allocated	3	4	4
Backing Store Map (Page → Block)			
Page 0	BS 0	BS 3	BS 7
Page 1	BS 1	BS 4	BS 8
Page 2	BS 2	BS 5	BS 9
Page 3		BS 6	BS 10
Page 4			
Page 5			
Page 6			
Page 7			

Inverted Page Table

Frame	Virtual Page #	PID	Valid Bit	Ref Word (Low = older)
0	2	1	T	2
1	3	2	T	1
2	-	-	F	-
3	1	0	T	3

Using your knowledge of demand paging, write down what will change in each of the data structures as each memory access is executed. Make changes to data structures as needed. **Remember that each command has a cumulative effect.** Report the effect of each read on the line provided. **Assume right thru' protocol for the memory writes.**

[5 points] PID 1: Write logical memory Address 10, 'B' _____

Main Memory

Address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents	O	T	O	N	G	F	U	N	-	-	-	-	A	D	*	F
Change																

Backing Store

Block	0	1	2	3	4	5	6	7	8	9	10
In Use?	T	T	T	T	T	T	T	T	T	T	T
Contents	THRE	AD*F	UNDO	RATE	*MON	OTON	ICCO	DEMA	ND*P	AGIN	GFUN
Change											

Inverted Page Table

Frame		VP #		PID		Valid Bit		Ref Word (Low = older)	
0		2		1		T		2	
1		3		2		T		1	
2		-		-		F		-	
3		1		0		T		3	

[5 points] PID 2: Read logical memory Address 10 _____

Main Memory

Address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents	O	T	O	N	G	F	U	N	-	-	-	-	A	D	*	F
Change																

Backing Store

Block	0	1	2	3	4	5	6	7	8	9	10
In Use?	T	T	T	T	T	T	T	T	T	T	T
Contents	THRE	AD*F	UNDO	RATE	*MON	OTON	ICCO	DEMA	ND*P	AGIN	GFUN
Change											

Inverted Page Table

Frame		VP #		PID		Valid Bit		Ref Word (Low = older)	
0		2		1		T		2	
1		3		2		T		1	
2		-		-		F		-	
3		1		0		T		3	

[5 points] PID 1: Read logical memory address 1_____

Main Memory

Address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents	O	T	O	N	G	F	U	N	-	-	-	-	A	D	*	F
Change																

Backing Store

Block	0	1	2	3	4	5	6	7	8	9	10
In Use?	T	T	T	T	T	T	T	T	T	T	T
Contents	THRE	AD*F	UNDO	RATE	*MON	OTON	ICCO	DEMA	ND*P	AGIN	GFUN
Change											

Inverted Page Table

Frame		VP #		PID		Valid Bit		Ref Word (Low = older)	
0		2		1		T		2	
1		3		2		T		1	
2		-		-		F		-	
3		1		0		T		3	

[5 points] PID 0: Write logical memory address 2, 'X' _____

Main Memory

Address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents	O	T	O	N	G	F	U	N	-	-	-	-	A	D	*	F
Change																

Backing Store

Block	0	1	2	3	4	5	6	7	8	9	10
In Use?	T	T	T	T	T	T	T	T	T	T	T
Contents	THRE	AD*F	UNDO	RATE	*MON	OTON	ICCO	DEMA	ND*P	AGIN	GFUN
Change											

Inverted Page Table

Frame		VP #		PID		Valid Bit		Ref Word (Low = older)	
0		2		1		T		2	
1		3		2		T		1	
2		-		-		F		-	
3		1		0		T		3	