

CSE 241 Digital Systems

Summer 2019

Course Description

A course in digital principles which includes the following topics: fundamentals of digital logic, number systems, codes, computer arithmetic, Boolean algebra, minimization techniques, basic components of digital circuits such as logic gates and flip-flops, design of combinational and sequential circuits, memory devices, and programming logic. Recommended for sophomore-level students.

Learning Outcomes

- Understand and apply Boolean Algebra
- Understand logic gates and their operation
- Understand Karnaugh maps and apply them to simplify logic expressions
- Understand signed and unsigned integer representation and arithmetic
- MSI circuit decoders, multiplexers and design of combinational circuits
- Flip-flops and sequential circuit synthesis
- Verilog hardware description language, synthesis and simulation

Course Prerequisites

None, however familiarity with using a computer is necessary. If you do not feel comfortable with word processors, web browsers, or general computing this course may not be appropriate at this time for you and you should speak with the instructor immediately.

Textbook and Materials

Required:

Textbook: The required textbook for this course is “Digital Design: Principles and Practice” 5th Edition, by John F. Wakerly. Pearson, 2017. ISBN-13: 978-0134460093, ISBN-10: 013446009X

Lab Kit: You will also buy a lab-kit of components customized for the course, there are two options. Do not buy both. If you choose not to buy a kit from Jameco, the list of components is below and you are expected to have them, and can purchase them from sources of your choice.

Option 1: You can buy at Jameco using one collective part number: 2244818
It costs \$25.42 + shipping and handling.

Option 2: The second part that we will use is an Arduino Uno. This is a very versatile and highly useful microcontroller board. This is often used in prototyping small circuits. You can buy both this option at Jameco using one collective part number: 2244800. If you purchase this kit you do not need to purchase the one above. It costs \$47.58 + shipping and handling.

Materials list:

<u>Part No.</u> <u>(at Jameco)</u>	<u>Qty.</u>	<u>Description</u>
2134993	1	830-Point Breadboard with 70-Piece Jumper Wire Kit Super Combo
46252	1	QUAD 2-INPUT POSITIVE NAND GATE DIP-14
46316	1	HEX INVERTER DIP-14
46375	1	QUAD 2-INPUT POSITIVE AND GATE DIP-14
48098	1	QUAD 2-INPUT EXCLUSIVE OR GATE DIP-14
46957	1	Quad D-Type Flip-Flop 16-Pin DIP
46607	1	3-TO-8 DECODER/DEMULTIPLEXER DIP-16
47466	1	QUAD 2-INPUT POSITIVE OR GATE DIP-14
333973	10	LED Uni-Color Red 660nm 2-Pin T-1 3/4 Box
34761	10	LED Uni-Color Green 565nm 2-Pin T-1 3/4
690620	20	0.25 Watt 100 Ohm Resistor Carbon Film 5%
222608	1	USB2.0 A/B Cable 3 Feet Black USB-A Male To USB-B Male
2258831	1	3-Pin SPDT Slide Switch
1586074	1	Pushbutton Tactile Switch SPST
2283495	1	Anti-Static Gel Wrist Strap
16838	1	IC Extractor Tool

Schedule

Lecture:

2-5:15 pm, MW, Clemons 19

Lab:

5:20-6:20 pm, MW, Bonner 114

Attendance

Lectures:

Students are required to attend lectures. The absence will risk missing of important content and information. In lecture activities should be expected every session and count towards your grade. If you do not show up for an exam or quiz without previous arrangements barring extreme unforeseeable circumstances, then you will not be allowed to make up the assignment.

Recitations/Labs:

If you complete your lab earlier than the full time assigned, attendance in the lab is not required. When labs are assigned it is mandatory that you attend your assigned lab section to perform your lab. Prelabs (if applicable) must be submitted prior to your assigned lab section as specified in the assignment. If you must miss your section, speak with your instructor as soon as possible. You are to use this time to work on your lab assignments however you may need to spend additional time outside of the lab to complete the work. You may also use this time to work on other course related assignments.

Instructor Contact Information

Dr. Jennifer Winikus

Email: jwinikus@buffalo.edu

Website: www.cse.buffalo.edu/~jwinikus

Office Phone: 716-645-4757

Office: Davis 351

Office Hours

By appointment

Academic Content

This is a tentative list of topics:

- Number Systems
- Signed Arithmetic
- Boolean Arithmetic
- Karnaugh Maps
- Combinational Logic
- Logic Gates
- Sequential Logic
- Verilog Design

Program Outcome Support:

Program Outcome Support

0: Not Supported, 1: Introduced, 2: Reinforced, 3: Mastered

CEN Program Outcome	1	2	3	4	5	6	7
Support Level	2	0	0	0	0	0	1

Mappings:

Course Learning Outcome	EAC 1	EAC 7	Assessment Type
Understand and apply Boolean Algebra	x	x	Homework, Labs, and Exams
Understand logic gates and their operation	x		Homework, Labs, and Exams
Understand Karnaugh maps and apply them to simplify logic expressions	x	x	Homework, Labs, and Exams
Understand signed and unsigned integer representation and arithmetic	x		Homework, Labs, and Exams
MSI circuit decoders, multiplexers and design of combinational circuits	x	x	Homework, Labs, and Exams
Flip-flops and sequential circuit synthesis	x	x	Homework, Labs, and Exams
Verilog hardware description language, synthesis and simulation	x	x	Homework, Labs, and Exams

Grading Policies

Your grade will be comprised of:

22.5 % Exam 1

32.5 % Final Exam

15 % Homework, Quizzes, and other assignments

30 % Laboratory Assignments*

Extra credit opportunities may be offered.

Your final score for the course will be converted into a letter grade as follows:

- A: 100–94
- A-: 93–90
- B+: 89–87
- B: 86–84
- B-: 83–80
- C+: 79–77
- C: 76–74
- C-: 73–70
- D+: 69–67
- D: 66–60
- F: 59–0

The instructor reserves the right to curve grades if appropriate and as they choose. Participation and attendance may be considered in the final grade assignment, with up to a 2% impact (which can be positive or negative).

*If you score less than 60% for the lab score for the term, you will fail the course independent of overall grade.

Incompletes (I/IU): The course follows the university undergraduate [incomplete](#) policy.

A grade of incomplete (“I”) indicates that additional coursework is required to fulfill the requirements of a given course. Students may only be given an “I” grade if they have a passing average in coursework that has been completed and have well-defined parameters to complete the course requirements that could result in a grade better than the default grade. An “I” grade may not be assigned to a student who did not attend the course.

Prior to the end of the semester, students must initiate the request for an “I” grade and receive the instructor’s approval. Assignment of an “I” grade is at the discretion of the instructor. Upon assigning an “I” grade, the instructor shall provide the student specification, in writing or by electronic mail, of the requirements to be fulfilled, and shall file a copy with the appropriate departmental office. Students must not re-register for courses for which they have received an “I” grade

Failure for Non-Attendance (FX): Students who have earned a failing grade due to lack of attendance (or participation where attendance is not applicable) will be awarded an “FX”.

Collaboration Policies

Unless explicitly told, all work is to be done independently with only the assistance of TAs and the instructor. You may discuss the general concepts of assignments and what the question asks for with other students but you must not discuss answers.

Unauthorized collaboration will result in an “F” in the course as a violation of academic integrity.

Exam Policy

There will be 2 exams.

- The first exam will have three parts: practice exam, traditional exam, and correction session.
 - Practice exam: is part of your assignment grade and is done in class the lecture prior to the traditional exam.
 - Traditional exam:
 - Correction session: 7-8 pm, and is *optional*. All accommodation requests for the correction session must be made a minimum of a week ahead of time. If you have accessibility resources accommodations for exams, please consult the instructor concerning what would be appropriate for your situation for the corrections session. Lecture will still be held that day.
- The final exam will have two parts: the practice exam and the traditional exam.
 - Practice exam is part of your assignment grade and is done in class on the last class of the term.
 - Traditional part of the exam is scheduled for the last lecture of the term, Wednesday, July

You can not borrow pens or pencils during the exam. During the exam there is to be no talking or looking at technology, doing so may result in an automatic “F” on the exam; and potentially in the course.

Any accommodations must be made in advanced barring extraordinary circumstances.

Due Dates

Late work:

No late work will be accepted. You have a 24 hour grace period after the due date where you can submit still at no penalty, after that close out, work will not be accepted.

No work will be accepted after midnight on the last day of classe barring extraordinary circumstances.

If a review of your assignment grading is desired, you have 1 week from the time the grade is released to request a review. Corrections are not allowed, with the exception of the special policies for exam 1 (these will be detailed further prior to the exam).

Submission Policy

All submissions will be made on UBLearns in PDF form unless otherwise instructed. Any assignment involving code, must be submitted typed. You will be instructed in lecture how to generate the appropriate files for submission of assignments containing code. Each file submitted must have your name and date printed clearly on the submission to be eligible for grading. Any file without your name and date or in a format other than instructed, will not be graded.

Email Policy

Students are responsible for email sent to their official University at Buffalo email address. Communication will not be done with non-university email addresses. A level of professionalism is expected with all communications. Make sure that you include “CSE241” in the subject line to support a timely response. Responses may be delayed outside of standard business hours and at other times you will be informed of.

Accessibility Resources

If you have any disability which requires reasonable accommodations to enable you to participate in this course, please contact the [Office of Accessibility Resources](#), 60 Capen Hall, 716-645-2608, and also the instructor of this course. The office will provide you with information and review appropriate arrangements for reasonable accommodations.

University Policies

You are expected to adhere to all university policies, including those listed below and not listed.

Academic Integrity Policy:

<https://catalog.buffalo.edu/policies/integrity.html>

Policy on Accommodations:

<https://www.buffalo.edu/administrative-services/policy1/ub-policy-lib/reasonable-accommodation.html>

The Office of Equity, Diversity and Inclusion provides many resources including the following policies to be followed:

Discrimination and Harassment:

<http://www.buffalo.edu/administrative-services/policy1/ub-policy-lib/discrimination-harassment.html>

Religious Accommodation and Expression:

<http://www.buffalo.edu/administrative-services/policy1/ub-policy-lib/religious-accommodation-expression.html>

Departmental Academic Integrity Policy:

<https://engineering.buffalo.edu/computer-science-engineering/undergraduate/resources-for-current-students/academic-integrity-students.html>

Student Code of Conduct:

<http://www.buffalo.edu/content/dam/www/studentlife/units/uls/student-conduct/ub-student-code-of-conduct.pdf>

Classroom Behavior Expectations:

<https://catalog.buffalo.edu/policies/obstruction.html>

Explanation of Grades:

<https://catalog.buffalo.edu/policies/explanation.html>

Departmental Statement on Academic Integrity in Coding Assignments and Projects

All academic work must be your own. Plagiarism, defined as copying or receiving materials from a source or sources and submitting this material as one's own without acknowledging the particular debts to the source (quotations, paraphrases, basic ideas), or otherwise representing the work of another as one's own, is never allowed. Collaboration, usually evidenced by unjustifiable similarity, is never permitted in individual assignments. Any submitted academic work may be subject to screening by software programs designed to detect evidence of plagiarism or collaboration.

It is your responsibility to maintain the security of your computer accounts and your written work. Do not share passwords with anyone, nor write your password down where it may be seen by others. Do not change permissions to allow others to read your course directories and files. Do not walk away from a workstation without logging out. These are your responsibilities. In groups that collaborate inappropriately, it may be impossible to determine who has offered work to others in the group, who has received work, and who may have inadvertently made their work available to the others by failure to maintain adequate personal security. In such cases, all will be held equally liable.

Departmental Policy on Violations of Academic Integrity

The CSE Department has a zero-tolerance policy for AI violation.

All AI violation cases will be reported to the department, school and university, and recorded. Even the 1st offense will receive "F" for the course, unless the instructor deems it appropriate to reduce the penalty.

Subsequent violation of AI in any form and in any other course will automatically result in a "F" grade, with no exception.

Copyright Policy

Materials used in connection with this course may be subject to copyright protection under Title 17 of the United States Code. Under certain Fair Use circumstances specified by law, copies may be made for private study, scholarship, or research. Electronic copies should not be shared with unauthorized users. If a user fails to comply with Fair Use restrictions, he/she may be liable for copyright infringement.

For more information on the SUNY policy of copyright ownership regarding materials in courses: <http://system.suny.edu/academic-affairs/faculty/faculty-ownership/>

Tentative Schedule

The schedule and content is subject to change. Please pay attention to announcements for details about important dates.

Lecture	Date	Material
1	W- 5/29	<ul style="list-style-type: none">• Introduction• Introduction to Digital Systems• Number Systems
2	M- 6/3	<ul style="list-style-type: none">• Arithmetic
3	W- 6/5	<ul style="list-style-type: none">• Switching Algebra• Logic Gates
4	M- 6/10	<ul style="list-style-type: none">• Logic Gates• Combinational Logic• Documentation and Fabrication Intro• Minimization• K-Maps
5	W- 6/12	<ul style="list-style-type: none">• More Gates• Time and Real World• Practice Exam
6	M- 6/17	<ul style="list-style-type: none">• Exam
7	W- 6/19	<ul style="list-style-type: none">• Verilog• MSI
8	M- 6/24	<ul style="list-style-type: none">• MSI• Sequential Logic
9	W- 6/26	<ul style="list-style-type: none">• Sequential Logic
10	M- 7/1	<ul style="list-style-type: none">• Device Wrap Up• Practice Exam
11	W- 7/3	<ul style="list-style-type: none">• Last class- Final Exam

Final exam is in lecture on the last day of classes, July 3rd.

Tentative Plan for Assignments:

You are anticipated to have 8 homework assignments, 9 labs, 1 design lab, 1 lab quiz, a lab practical, and two practice exam activities. This is subject to change and assignments may be added or removed.

Important Dates

First Day of Classes: Wednesday, May 29

Last Day to Drop/Add: Thursday, May 30

Last Day to Resign: Monday, June 24

Last Day of Classes: Wednesday, July 3

All content in the syllabus is subject to change based on the needs of the class and the discretion of the instructor