

Reading and Exercises:

In addition to ALR chapter 29 section 4 and the Barrington-Maciel “Advanced” lectures, please read the following entry in Richard Lipton’s weblog:

<http://rjlipton.wordpress.com/2010/03/08/a-class-of-graph-properties-computable-in-linear-time/> for examples of logical formulas.

This is a “short” problem set, with some things I realized are useful to assign during my lectures.

(1) Suppose C is a leveled circuit of depth d . Define the *width* w to be the maximum total fan-in of gates in any one level—i.e. the total number of input wires for that level. Then the size s is at most dw . Suppose every gate in C has fan-in at most 2.

Create an equivalent leveled circuit C' such that every gate in C' also has fan-out at most 2. Does the depth d change? Define a bound on the new width w' . (Note that “equivalent” technically means that for all $x \in \{0, 1\}^n$, $C'(x) = C(x)$, where C and C' have the same number n of input gates, but the term usually connotes that C' simulates C in some overt manner. 12 pts.)

(2) What happens to circuits of size $s(n)$ and depth $d(n)$ and fan-in and fan-out 2 when you convert them into equivalent formulas by recursively duplicating gates that have 2 output wires? State the new size and depth, and what they become when you start with NC^1 circuits of bounded fan-out.

Then work out what happens when the fan-out and/or the fan-in is unbounded, i.e., bounded only by the number of gates in the original circuit. Note that when just the fan-out is unbounded, you can use problem (1). What happens when $d(n)$ is constant? and when $d(n) = \log n$? (24 pts. total)

(3) Find a polynomial f that represents $\text{MAJ}(x_1, x_2, x_3, x_4, x_5)$ over Z_2 , i.e. takes value 0 when and only when at least three inputs are 1. Then do the same over Z_3 , and answer whether you can get any savings in degree or size from using a weak representation (i.e., allowing the value 2 on inputs with two or fewer 1's) instead of a strong one. (21 pts., for 57 total)