CSE 490/590 Computer Architecture, Spring 2024

Appendix 2 – Creating and Using a Project with Vivado

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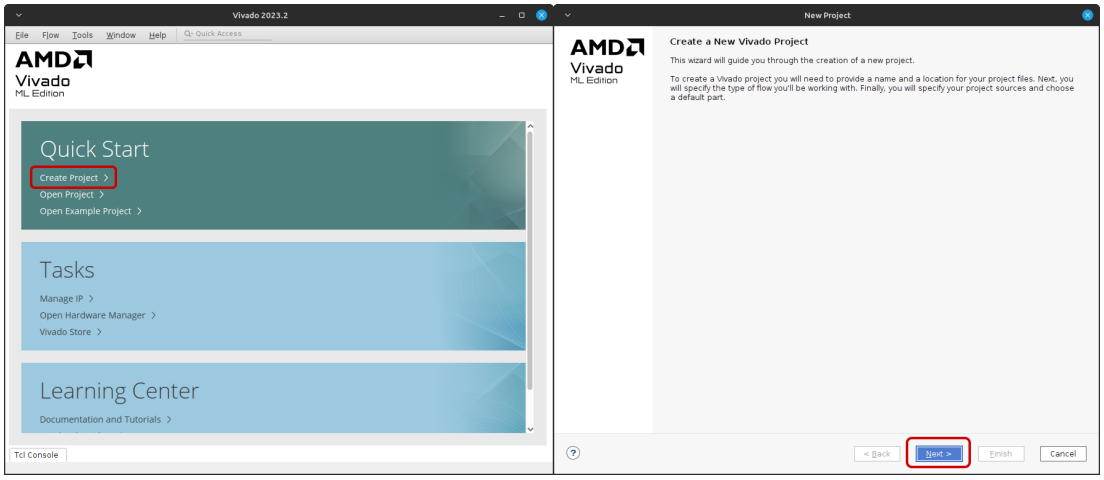
1 - Creating a Project

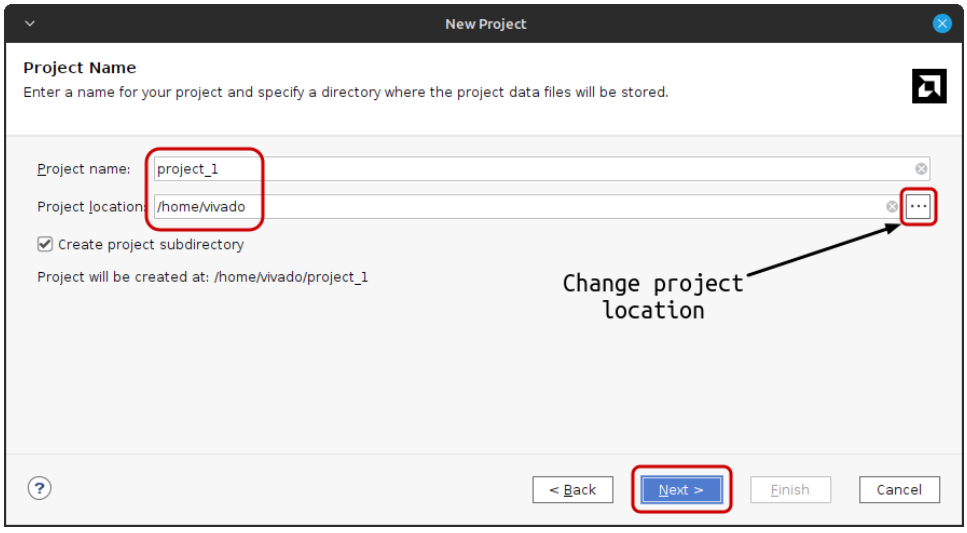
Step 1.1:

Click on the “Create Project” button and then hit “Next”.



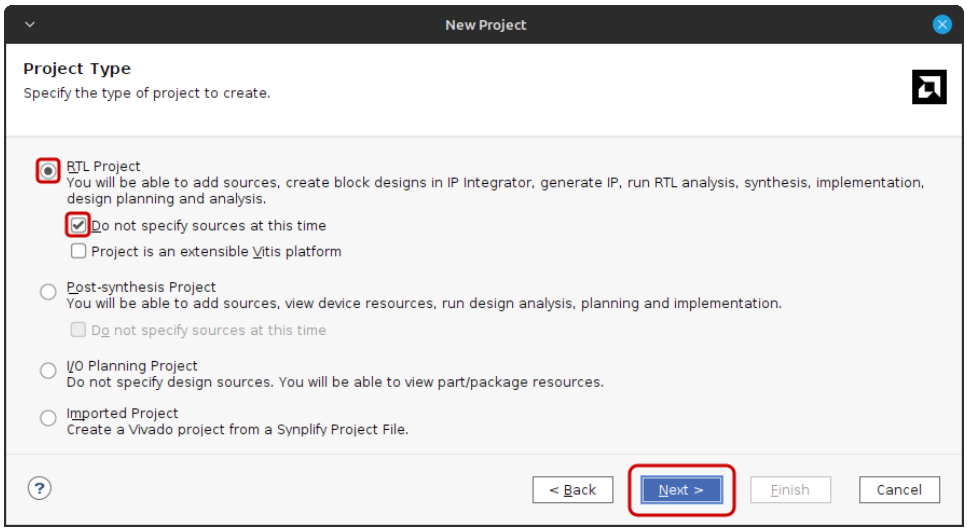
Step 1.2:

Name your project and specify a particular path. Make sure the project path location does not have spaces. You can control where the project is saved by clicking on the three dots at the end of the project location box and selecting the folder (or making a new folder) where you want your project to be saved. **Make sure you know where you saved your project, so you can send your files to your teammates throughout the process.**



Step 1.3:

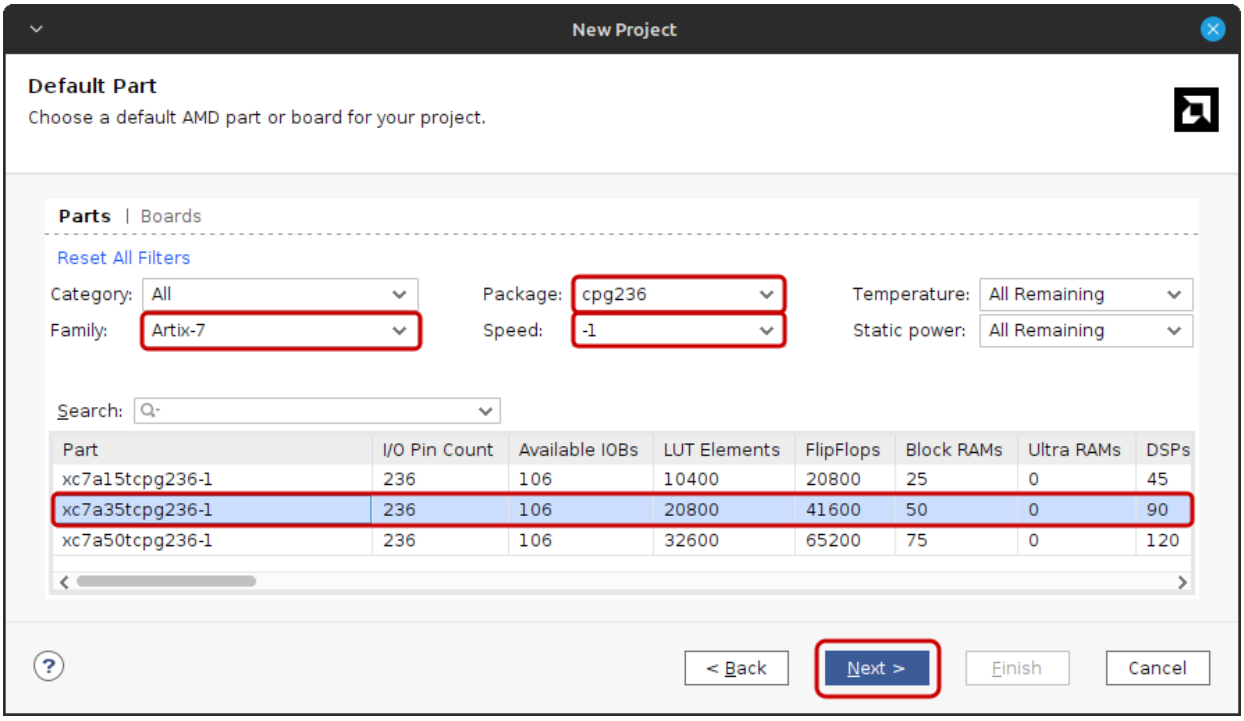
Choose “RTL Project” and check the box which says “Do not specify sources at this time”.



Step 1.4:

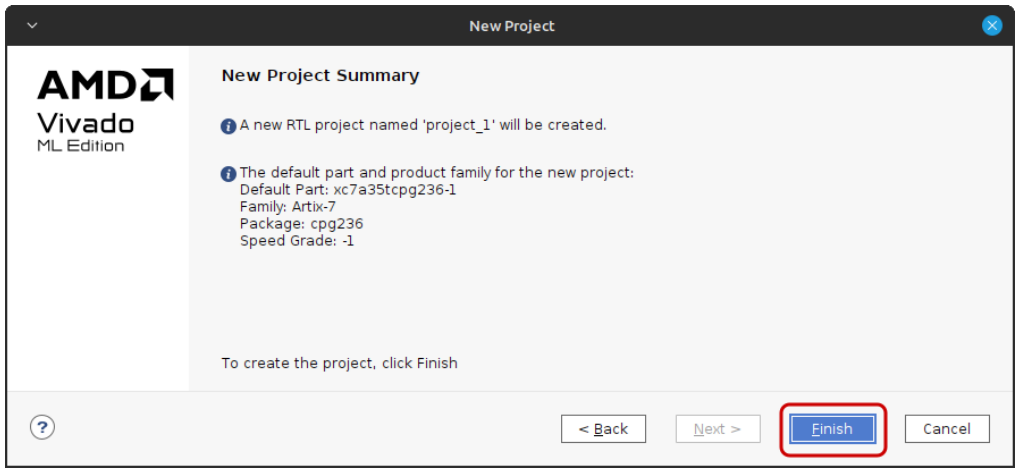
The Basys 3 FPGA board uses an Artix 7 FPGA. From the datasheet and user manual, select all the specific options as shown below.

(Family: Artix-7, Package: cpg236, Speed: -1, Part: xc7a35tcpg236-1)



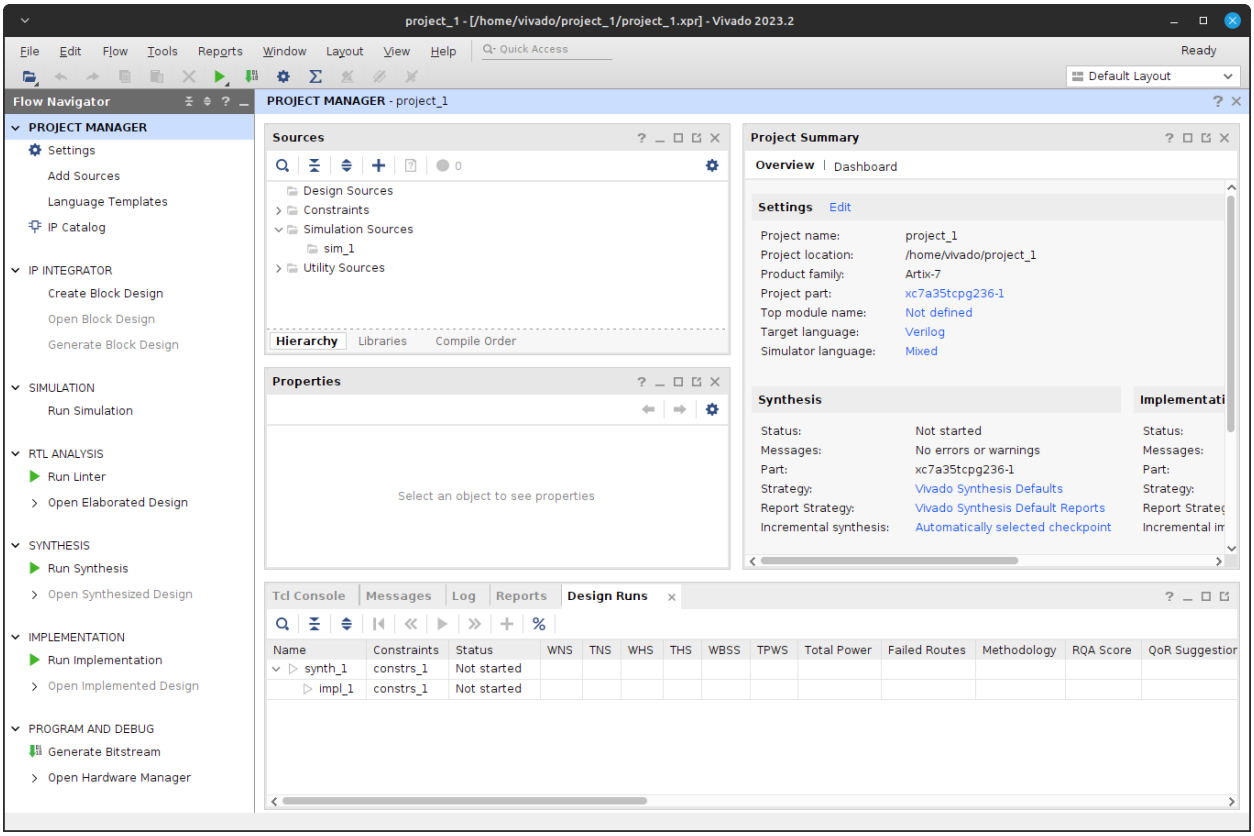
Step 1.5:

Click finish. Creating the project may take a few seconds.



Step 1.6:

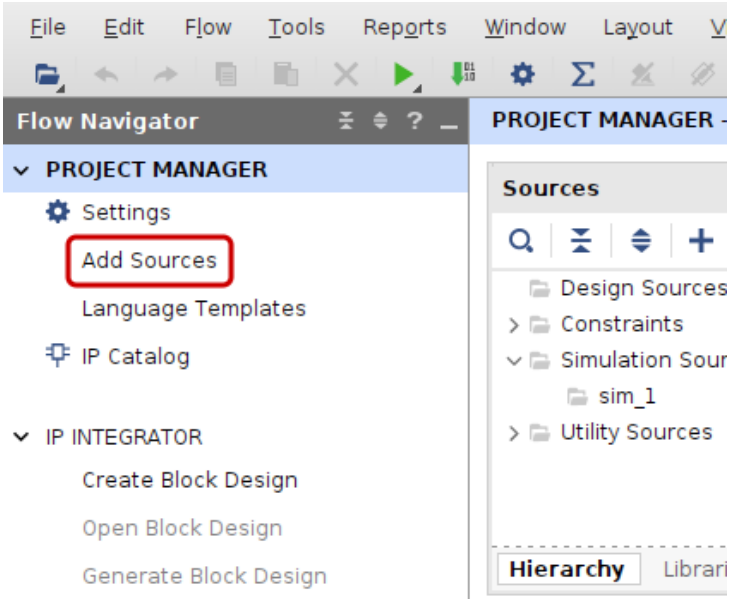
Make sure your project manager looks like this:



2 - Adding Sources to the Project

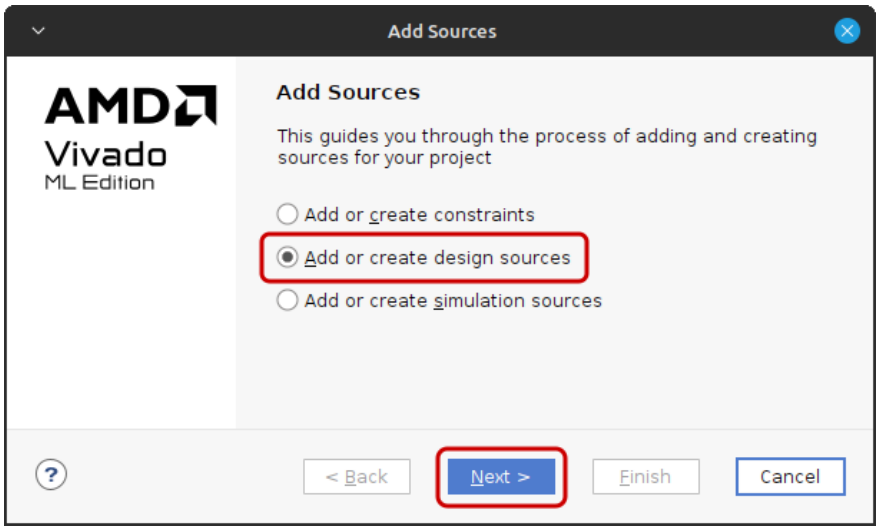
Step 2.1:

To add your first Verilog code, click ‘Add Sources’



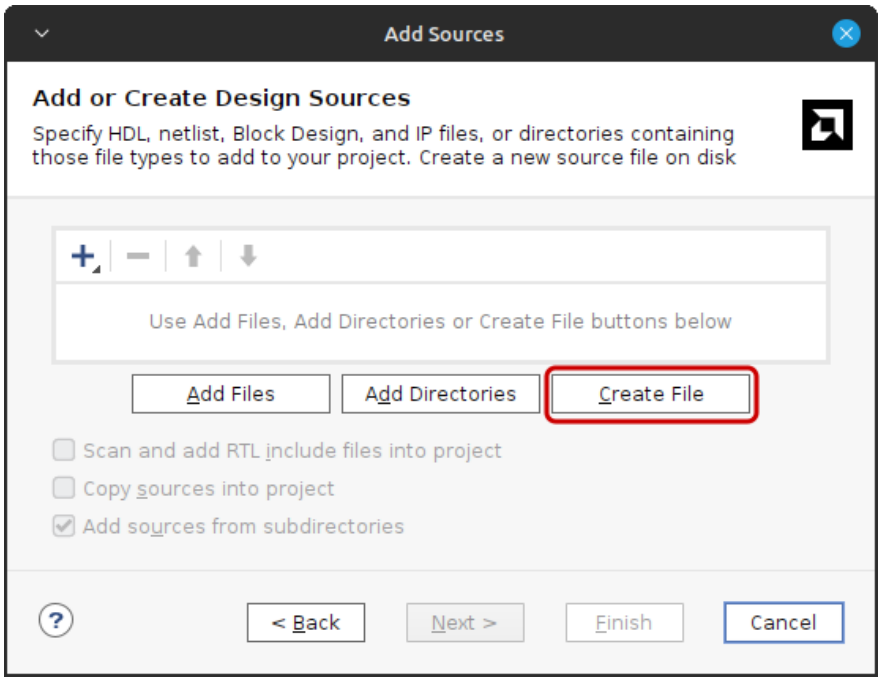
Step 2.2:

Click on ‘Add or create design sources’.



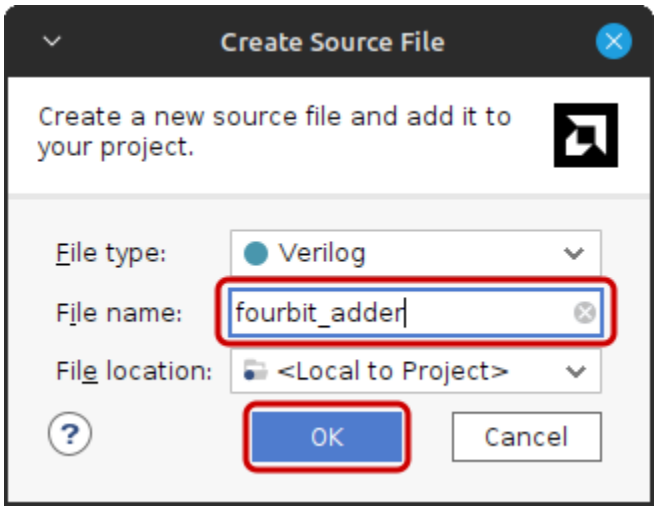
Step 2.3:

If your Verilog code (.v) has already been created, click ‘Add files’ and browse to select the corresponding file. If you need to create a new Verilog code, click ‘Create file’.



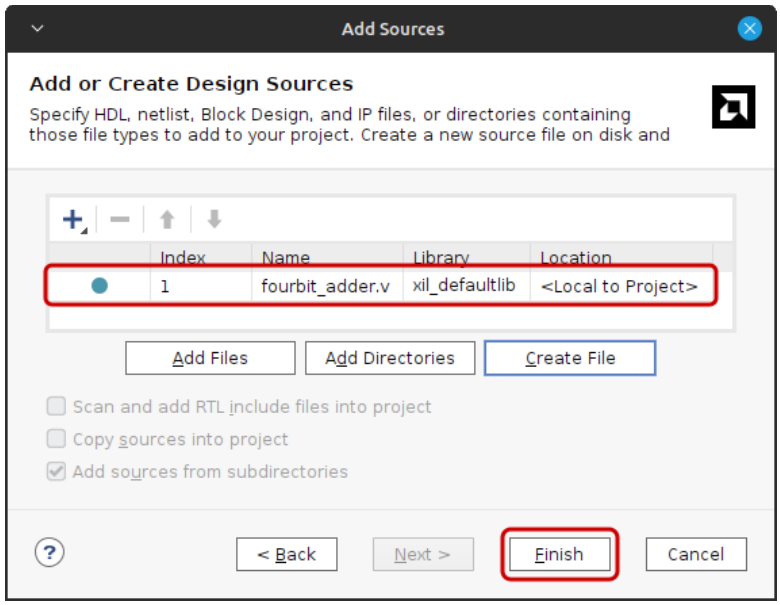
Step 2.4:

Name the file and hit ‘OK’.



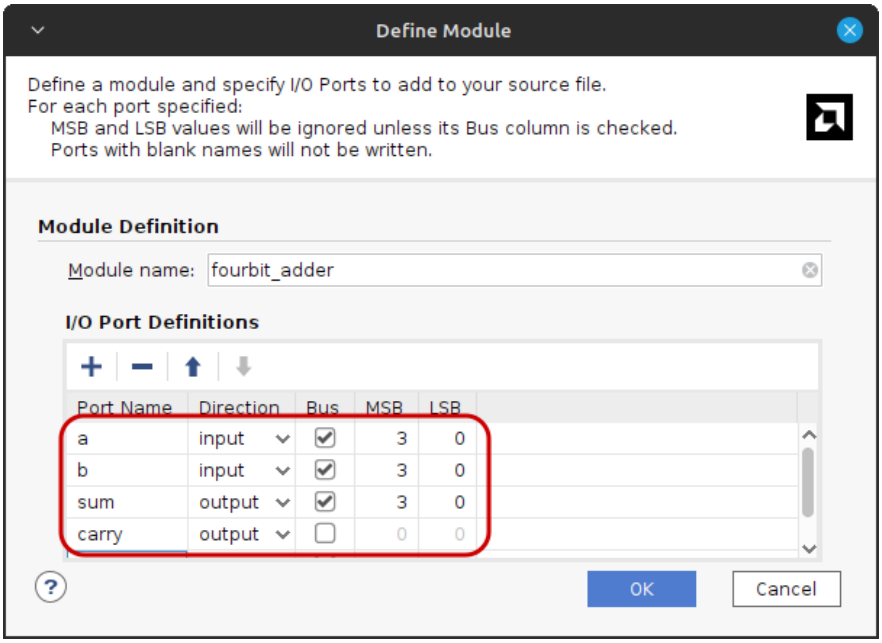
Step 2.5:

This is an example for a 4-bit adder, so there is only one Verilog file created here. In case of the 8-bit cpu, a Verilog file has to be created for each component. Click ‘Finish’. You can add other sources later as well.



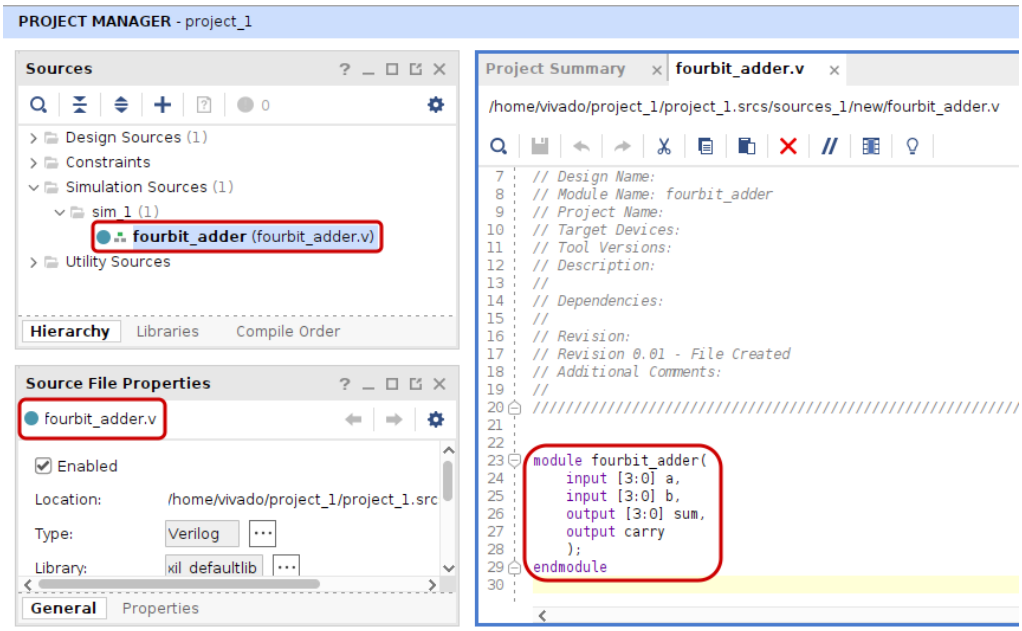
Step 2.6:

Define the input and output ports and bus width if the ports are more than a bit wide. This step is optional. You can hit 'Cancel' and decide on how many ports you need as you write the code.



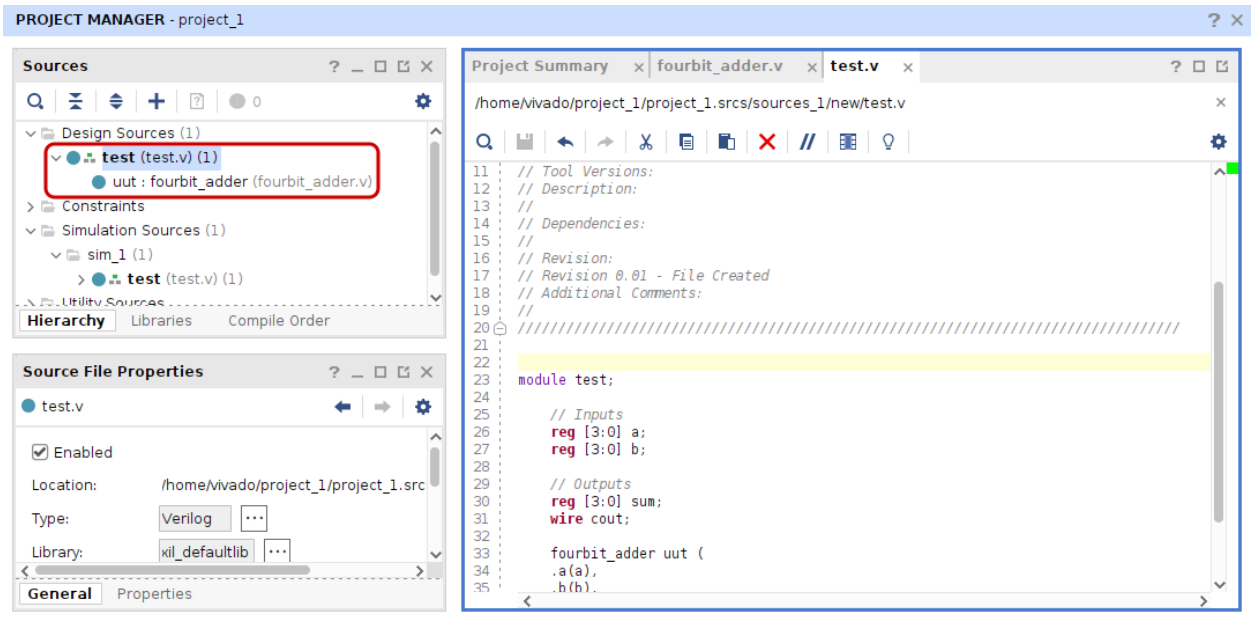
Step 2.7:

This is what your project manager should look like.



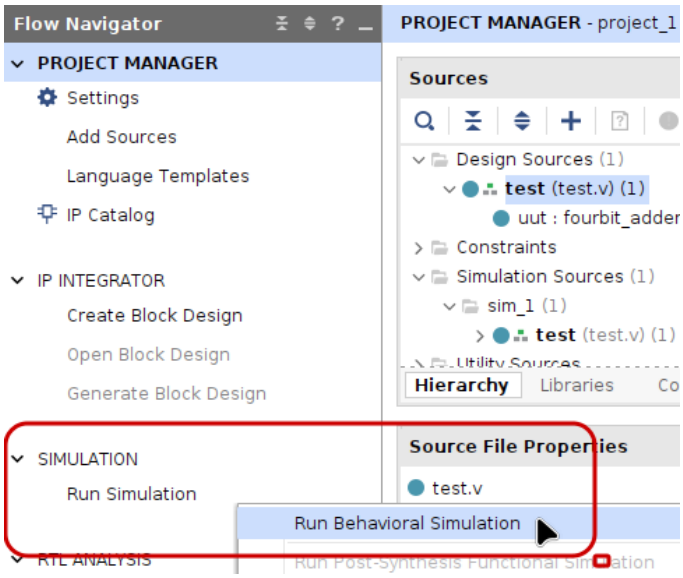
Step 2.8:

Repeat Steps 2.1 through 2.7 to create a Verilog test bench that tests the design of the four-bit adder code with various test cases.



Step 2.9:

The test bench can then be simulated by selecting ‘Run Simulation’ and then ‘Run behavioral simulation’ in the Project manager.


Flow Navigator
PROJECT MANAGER
Settings
Add Sources
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IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
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RTL ANALYSIS
PROJECT MANAGER - project_1
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test (test.v) (1)
uut : fourbit_adder
Constraints
Simulation Sources (1)
sim_1 (1)
test (test.v) (1)
Hierarchy
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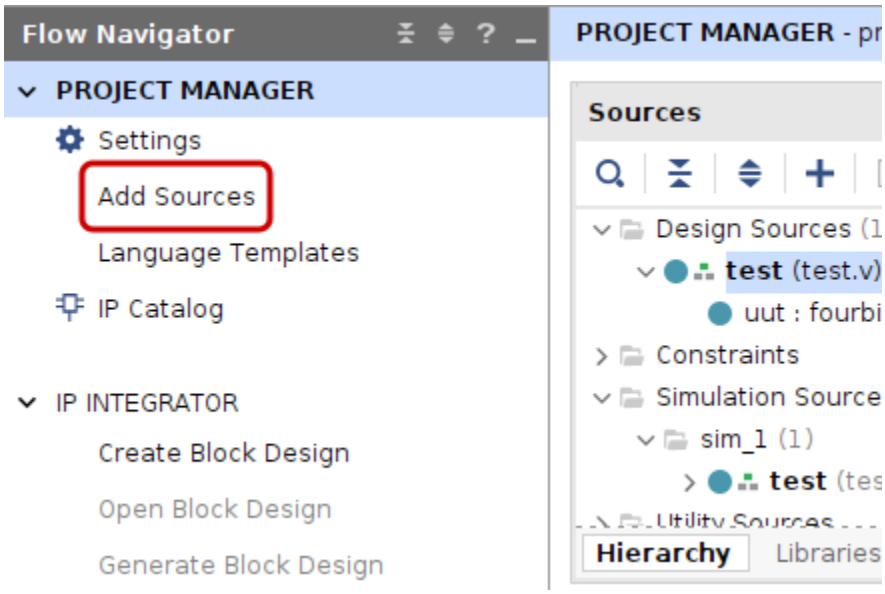
Source File Properties
test.v
Run Behavioral Simulation

3 - Generating a Bitstream File

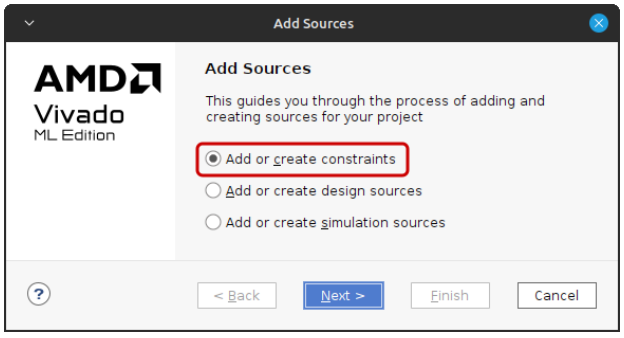
Step 3.1:

Add a constraints file (Constraints are a combination of industry standard Synopsys Design Constraints (SDC version 1.9) and Xilinx proprietary physical constraints.). In the project manager window select ‘Add sources’.



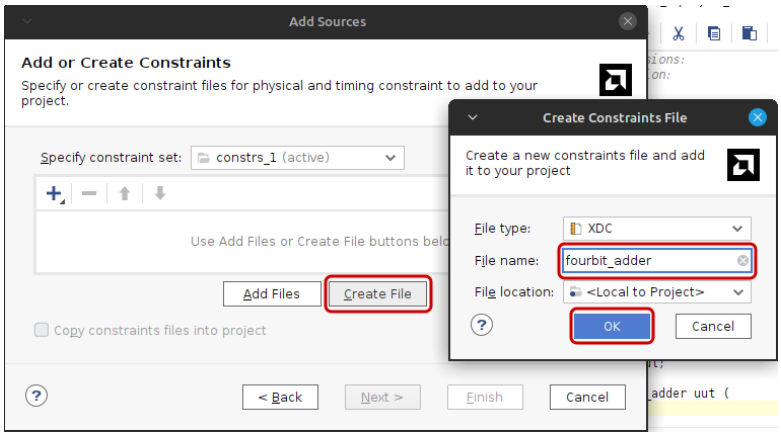
Step 3.2:

Click Add or Create constraints.



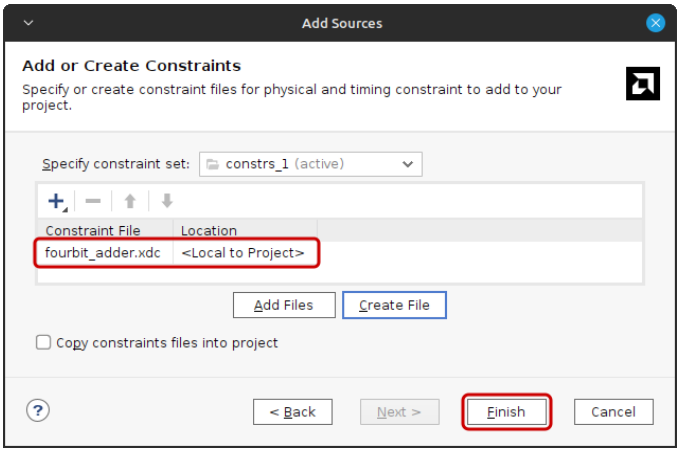
Step 3.3:

Select Create file and give a name to the constraint file.



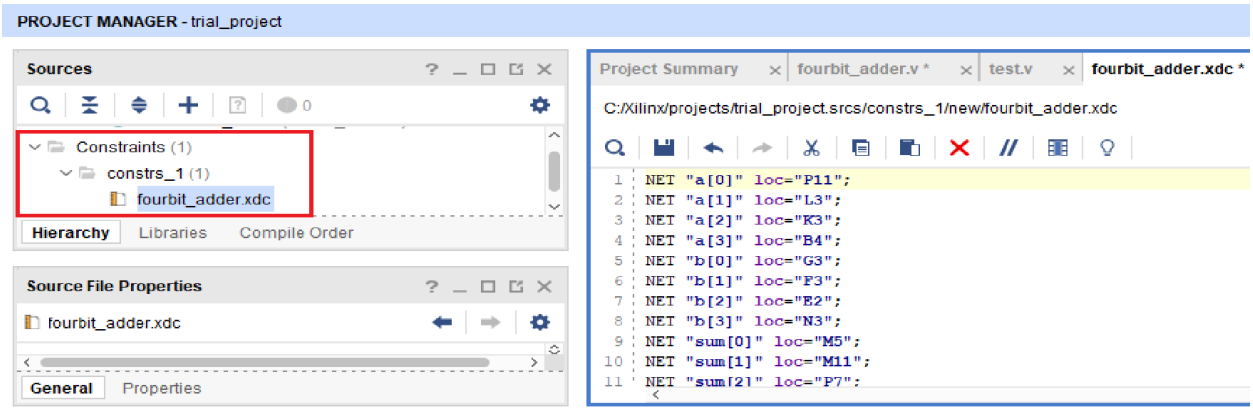
Step 3.4:

<filename>.xdc will be created. Click the 'Finish' button.



Step 3.5:

The sources tab will have the constraint file as shown. You can edit this file to map the inputs and outputs of the processor to switches and push buttons on the FPGA board.



Step 3.6:

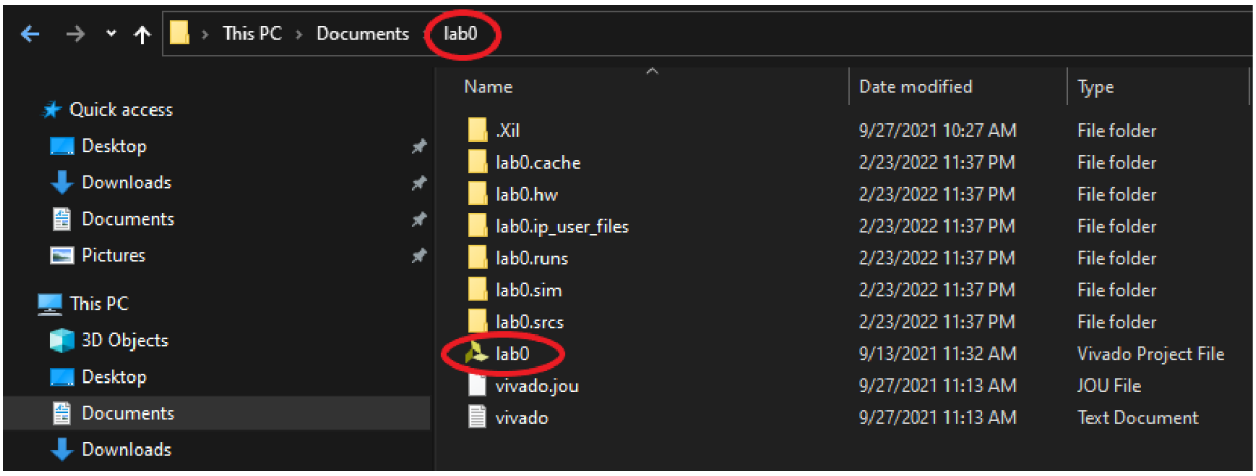
Click on the 'Run Synthesis' option in the Project Manager window, then

click on the 'Run Implementation' option in the Project Manager window, then

click on the ‘Generate Bitstream’ option in the Project Manager window.

4 - Sharing Project Files with Teammates

Throughout the project you will send your code or your entire project to your teammates. Keep track of where you saved your project. When you want to send your project to someone else, locate your project file folder. You will need to compress and zip the entire folder that contains the project subfolders such as .srcs, .cache, .sim, etc., (in this case, the folder “lab0”):



When running a project which you have received, make sure to extract the project folder first. From the extracted folder, double click the file with the Vivado logo and listed as type “Vivado Project File” to open the project in Vivado. (If the project folder is being viewed on a computer that does not have Vivado installed, this file will be listed as type “XPR file.”)

If you are running Vivado remotely, you will need to open the project from within the Vivado GUI. From the start-up menu, click on “Open Project” and use the Vivado file manager to find your project folder and double click on the XPR file: