CSE 490/590 Computer Architecture, Spring 2024 Appendix 2 – Creating and Using a Project with Vivado

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1 - Creating a Project

Step 1.1:

Click on the "Create Project" button and then hit "Next".

 Vivado 2023.2 	- • 8 ×		New Project 📀
Efe Flow Tods Window Help Q-OwinkArcess		AMD Vivado ML Edition	Create a New Vivado Project This stard will guide you through the creation of a new project. To create a Vivado project you will need to prode a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
Quick Start Create Project > Open Project > Open Example Project >	Î		
Tasks Manage (P > Open Hardware Manager > Vivado Store >			
Learning Center Documentation and Tutorials >		?	- Back Boot Swith Cancel

Step 1.2:

Name your project and specify a particular path. Make sure the project path location does not have spaces. You can control where the project is saved by clicking on the three dots at the end of the project location box and selecting the folder (or making a new folder) where you want your project to be saved. Make sure you know where you saved your project, so you can send your files to your teammates throughout the process.

~	New Project	8
Project Name Enter a name for your project and specify a directory	where the project data files will be stored.	
Project name: Project location /home/vivado ✓ Create project subdirectory Project will be created at: /home/vivado/project_1	Change project location	
•	Seack Next > Einish	Cancel

Step 1.3:

Choose "RTL Project" and check the box which says "Do not specify sources at this time".

~	New Project 🔗
Proj Spec	ify the type of project to create.
١	RTL Project You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis. Poject is an extensible <u>V</u> itis platform
С	Post-synthesis Project You will be able to add sources, view device resources, run design analysis, planning and implementation. Do not specify sources at this time
C	UO Planning Project Do not specify design sources. You will be able to view part/package resources. Imported Project Create a Vivado project from a Synplify Project File.
?	< Back Einish Cancel

Step 1.4:

The Basys 3 FPGA board uses an Artix 7 FPGA. From the datasheet and user manual, select all the specific options as shown below.

(Family: Artix-7, Package: cpg236, Speed: -1, Part: xc7a35tcpg236-1)

			New Proj	ect				8
efault Pa hoose a de	art Ifault AMD part (or board for your project.						ת
Parts	Boards							
Reset All	Filters							
Category:	All	✓ Pa	ckage: cpg236	~	Tem	perature:	All Remaining	~
Family:	Artix-7	❤ Sp	eed: -l	~	Stati	c power:	All Remaining	~
<u>S</u> earch:	Q-	~						
Part		I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RA	Ms Ultra RAMs	DSPs
xc7a15t	cpg236-1	236	106	10400	20800	25	0	45
xc7a35to	cpg236-1	236	106	20800	41600	50	0	90
xc7a50to	cpg236-1	236	106	32600	65200	75	0	120
<								>
?				< <u>B</u> ack	<u>N</u> ext	>	Einish	Cancel

Step 1.5:

Click finish. Creating the project may take a few seconds.

~	New Project 😵
	New Project Summary
Vivado ML Edition	A new RTL project named 'project_1' will be created.
	The default part and product family for the new project: Default Part: xc7a35tcpg236-1 Family: Artix-7 Package: cpg236 Speed Grade: -1
	To create the project, click Finish
?	< Back Next > Einish Cancel

Step 1.6:

Make sure your project manager looks like this:



2 - Adding Sources to the Project

Step 2.1:

To add your first Verilog code, click 'Add Sources'



Step 2.2:

Click on 'Add or create design sources'.

~	Add Sources 🛛 😵
AMD Vivado ML Edition	Add Sources This guides you through the process of adding and creating sources for your project Add or create constraints Add or create design sources Add or create simulation sources
?	< <u>B</u> ack <u>Einish</u> Cancel

Step 2.3:

If your Verilog code (.v) has already been created, click 'Add files' and browse to select the corresponding file. If you need to create a new Verilog code, click 'Create file'.

~		Add Sources		8
Add or Specify H those file	Create Design So IDL, netlist, Block Desi types to add to your	purces gn, and IP files, or dir project. Create a new	ectories containing v source file on disk	2
+,	─ ↑ ↓ Use Add Files, Add	Directories or Create	File buttons below	
	Add Files	A <u>d</u> d Directories	<u>C</u> reate File	
☐ Sca ☐ Cop ✔ Add	n and add RTL <u>i</u> nclude y <u>s</u> ources into project so <u>u</u> rces from subdire	e files into project ectories		-
?	< <u>B</u> ack	<u>N</u> ext >	Einish	Cancel

Step 2.4:

Name the file and hit 'OK'.



Step 2.5:

This is an example for a 4-bit adder, so there is only one Verilog file created here. In case of the 8-bit cpu, a Verilog file has to be created for each component. Click 'Finish'. You can add other sources later as well.

~		Add So	urces	8
Add or Cre Specify HDL, r those file type	e ate Desig netlist, Block es to add to	n Sources Design, and IP file your project. Crea	s, or directorie te a new source	s containing e file on disk and
+, -	+ +			
	Index	Name	Library	Location
•	1	fourbit_adder.v	xil_defaultlib	<local project="" to=""></local>
☐ Scan an ☐ Copy <u>s</u> oi ✔ Add so <u>u</u>	<u>A</u> dd Files d add RTL <u>i</u> n urces into pr rces from su	A <u>d</u> d Direc clude files into pro roject bdirectories	ject	<u>C</u> reate File
?	[< <u>B</u> ack	Next >	<u>F</u> inish Cancel

Step 2.6:

Define the input and output ports and bus width if the ports are more than a bit wide. This step is optional. You can hit 'Cancel' and decide on how many ports you need as you write the code.

~	Define Module	8
Define a module For each port sp MSB and LSB v Ports with blar	and specify I/O Ports to add to your source file. ecified: ralues will be ignored unless its Bus column is checked. nk names will not be written.	2
Module Defini	tion	
<u>M</u> odule nam	e: fourbit_adder	8
I/O Port Def	finitions	
+ -	↑ ↓	
Port Name	Direction Bus MSB LSB	
a	input 🗸 🗹 3 0	^
b	input 🗸 🗹 3 0	
sum	output 🗸 🖌 3 0	
carry	output 🗸 🗌 0 0	~
?	ОК	Cancel

Step 2.7:

This is what your project manager should look like.

PROJECT MANAGER - project_1	
Sources ? _ D 🗄 ×	Project Summary × fourbit_adder.v ×
Q ¥ ≑ + 2 ● 0 🌣	/home/vivado/project_1/project_1.srcs/sources_1/new/fourbit_adder.v
<pre>> Design Sources (1) > Design Sources (1) > Design Sources (1) > Design Sources (1) > Design 1 (1) Design 1 (1) > Design 1 (1) </pre>	Q IIII ▲ X III III Q 7 // Design Name: A IIII X IIII Q 8 // Module Name: fourbit_adder 9 // Project Name: Q IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII
Hierarchy Libraries Compile Order Source File Properties ? _ □ □ □ ×	14 // Dependencies: 15 // 16 // Revision: 17 // Revision 0.01 - File Created 18 // Additional Comments: 19 //
● fourbit_adder.v ← → 🌣	20 ≙ ///////////////////////////////////
Enabled Location: /home/vivado/project_1/project_1.src Type: Verilog Library: kil defaultlib	22 23 module fourbit adder(194 25 input [3:0] a, 25 input [3:0] b, 0 utput [3:0] sum, 0 utput carry 28 29 endmodule 30
General Properties	<

Step 2.8:

Repeat Steps 2.1 through 2.7 to create a Verilog test bench that tests the design of the four-bit adder code with various test cases.



Step 2.9:

The test bench can then be simulated by selecting 'Run Simulation' and then 'Run behavioral simulation' in the Project manager.

Flow Navigator	≭ ≑ ? _	PROJECT MANAGER - project_1	
✓ PROJECT MANAGER		Sources	
🔅 Settings			
Add Sources			
Language Templates		V Design Sources (1)	
IP Catalog		v • test (test.v) (1)	
T in Catalog		> Constraints	
V IP INTEGRATOR		✓ Simulation Sources (1)	
Create Block Design		∨ 🚍 sim_l (1)	
Open Plack Design			
open block besign		Hierarchy Libraries Co	
Generate Block Desig	n	incluring Eistance co	
		Source File Properties	
Run Simulation		test.v	
	Run Behav	ioral Simulation	
RTL ANALYSIS	Run Post-Synthesis Functional SimDation		

3 - Generating a Bitstream File

Step 3.1:

Add a constraints file (Constraints are a combination of industry standard Synopsys Design Constraints (SDC version 1.9) and Xilinx proprietary physical constraints.). In the project manager window select 'Add sources'.

Flow Navigator	≭ ≑ ? _	PROJECT MANAGER - pr	
✓ PROJECT MANAGER		Sources	
Add Sources		Q ₹ ≑ + [
Language Templates		Design Sources (1 > • • • • test (test.v)	
₽ IP Catalog		 uut : fourbi Constraints 	
✓ IP INTEGRATOR		∨ □ Simulation Source	
Create Block Design		✓ □ sim_1 (1)	
Open Block Design		> 📑 test (tes	
Generate Block Design	n	Hierarchy Libraries	

Step 3.2:

Click Add or Create constraints.



Step 3.3:

Select Create file and give a name to the constraint file.



Step 3.4:

<filename>.xdc will be created. Click the 'Finish' button.

Add Sources				
Add or Create Constraints Specify or create constraint files for physical and timing constraint to add to your project.				
<u>S</u> pecify constrai	nt set: 🕞 constrs_1 (active) 🗸			
$ +_{a} = + $	+			
Constraint File	Location			
fourbit_adder.x	ic <local project="" to=""></local>			
	Add Files			
□ Copy constraints files into project				
?	< Back Next > Einish Cancel			

Step 3.5:

The sources tab will have the constraint file as shown. You can edit this file to map the inputs and outputs of the processor to switches and push buttons on the FPGA board.

PROJECT MANAGER - trial_project		
Sources	? _ 🗆 🖒 ×	Project Summary × fourbit_adder.v* × test.v × fourbit_adder.xdc*
Q 素 ≑ + ? ● 0	0	C:/Xilinx/projects/trial_project.srcs/constrs_1/new/fourbit_adder.xdc
✓ ☐ Constraints (1)	^	Q ₩ ♠ ≁ X ₪ ₪ X // Ⅲ Ω
✓ Constrs_1 (1) ☐ fourbit adder xdc		1 NET "a[0]" loc="P11"; 2 NET "a[1]" loc="L3";
Hierarchy Libraries Compile Order		3 NEI "a[2]" loc="K3"; 4 NEI "a[3]" loc="B4";
		5 NET "b[0]" loc="G3";
Source File Properties	? _ O G X	7 NET "b[2]" loc="E2";
l fourbit_adder.xdc	← → Q	8 NET "b[3]" loc="N3";
< <		<pre>9 NE1 "Sum[0]" 10C="M5"; 10 NET "sum[1]" loc="M11";</pre>
General Properties		11 ' NET "sum[2]" loc="P7":

Step 3.6:

Click on the 'Run Synthesis' option in the Project Manager window, then

click on the 'Run Implementation' option in the Project Manager window, then

click on the 'Generate Bitstream' option in the Project Manager window.



4 - Sharing Project Files with Teammates

Throughout the project you will send your code or your entire project to your teammates. Keep track of where you saved your project. When you want to send your project to someone else, locate your project file folder. You will need to compress and zip the entire folder that contains the project subfolders such as .srcs, .cache, .sim, etc., (in this case, the folder "lab0"):

$\leftarrow \rightarrow \checkmark \uparrow$ $\square \rightarrow$ This PC \rightarrow Documents (lab)								
	Nar	me	Date modified	Туре				
📌 Quick access		VII	0/37/2021 10-37 AM	File felder				
💻 Desktop	* -		9/21/2021 T0:27 AM	File folder				
Downloade		lab0.cache	2/23/2022 11:37 PM	File folder				
		lab0.hw	2/23/2022 11:37 PM	File folder				
🚆 Documents	* 📑	lab0.ip_user_files	2/23/2022 11:37 PM	File folder				
Pictures	* 🔒	lab0.runs	2/23/2022 11:37 PM	File folder				
This PC		lab0.sim	2/23/2022 11:37 PM	File folder				
		lab0.srcs	2/23/2022 11:37 PM	File folder				
🜉 3D Objects	A	lab0	9/13/2021 11:32 AM	Vivado Project File				
E Desktop		vivado.jou	9/27/2021 11:13 AM	JOU File				
🚆 Documents		vivado	9/27/2021 11:13 AM	Text Document				
🖊 Downloads								

When running a project which you have received, make sure to extract the project folder first. From the extracted folder, double click the file with the Vivado logo and listed as type "Vivado Project File" to open the project in Vivado. (If the project folder is being viewed on a computer that does not have Vivado installed, this file will be listed as type "XPR file.")

If you are running Vivado remotely, you will need to open the project from within the Vivado GUI. From the start-up menu, click on "Open Project" and use the Vivado file manager to find your project folder and double click on the XPR file:

