## Appendix 3 Programming the Basys 3 FPGA board

If you are running the Vivado locally then follow the steps

1. After successful completion of the Bitstream Generation, select Open Hardware manager from the dialog box or Flow -> Open Hardware Manager

| Bitstream Generation Completed               |  |  |  |  |
|--|--|--|--|--|
| Bitstream Generation successfully completed. |  |  |  |  |
| ◯ <u>V</u> iew Reports                       |  |  |  |  |
| Open Hardware Manager                        |  |  |  |  |
| O Generate Memory Configuration File         |  |  |  |  |
|  |  |  |  |  |
| OK Cancel                                    |  |  |  |  |

- 2. Connect the FPGA board to your laptop
- 3. Click on Open target and select Auto connect. Now you will be connected to the FPGA board



4. Now Click on Program Device in the Hardware Manager window. Select the bit file and hit Program HARDWARE MANAGER - localhost/xilinx\_tct//Digilent/210183794310A

| 1 There are no debug cores. Program device | ce Refresh devic | e   |
|--|------------------|---|
| Hardware ?                                 | _ 🗆 🖒 ×          | fourbit_adder.v   |
| Q   素   ♦   ∅   ▶   ≫   ■                  | ٥                | C:/Xilinx/projects/trial_project.srcs/sources_1/new/fourbit_adder.v |
| Name                                       | Status           |   |
| V localhost (1)                            | Connected ^      |   |
| ✓ ■ xilinx_tcf/Digilent/2101837943         | Open 🗸           | 21 22   |

|  |  | ×   |
|--|--|---|
| gramming file and download it to your hardware device. You can opti<br>file that corresponds to the debug cores contained in the bitstream | onally   | 4   |
| C:/Xilinx/projects/trial_project.runs/impl_1/fourbit_adder.bit   | 8  |   |
|  |  |   |
| startup check  |  |   |
|  |  |   |
| Program  | Cano   | el  |
|  | gramming file and download it to your hardware device. You can opti-<br>file that corresponds to the debug cores contained in the bitstream<br>C:/Xilinx/projects/trial_project.runs/impl_1/fourbit_adder.bit<br>startup check | gramming file and download it to your hardware device. You can optionally<br>file that corresponds to the debug cores contained in the bitstream<br>C:/Xilinx/projects/trial_project.runs/impl_1/fourbit_adder.bit<br>startup check |

If you are running the Vivado on the CSE server then do the following

1. Download the hardware server on your local machine from

https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-designtools/archive.html (This is not the complete software and just requires approx.. ~400MB and download time of few minutes)

2. Run the xsetup file

3. Run the hardware server from C:\Xilinx\HWSRVR\2019.2\bin\hw\_server.bat. You will see the following window



- 4. Open Hardware manager from the dialog box or Flow -> Open Hardware Manager
- 5. Connect the FPGA board to your laptop
- 6. Click on Open target and select Open New Target.

| No hardware target is open. | Ope | n target                    |   |
|-----------------------------|-----|-----------------------------|---|
| Hardware                    | ø   | Auto Connect                |   |
| 2,   ≚   ≑   Ø   ▶   >      | >   | Available Targets on Server | 2 |
| No conter                   |     | Open New Target             |   |

7. Click on Next in the Open New Hardware Target Wizard

| λ.           | Open New Hardware Target   | • • ×  |  |  |  |  |
|--------------|--|--------|--|--|--|--|
|              | Open Hardware Target   |        |  |  |  |  |
| HLx Editions | This wizard will guide you through connecting to a hardware target.  |        |  |  |  |  |
|              | To connect to a remote hardware target, provide the host name and IP port of the remote machine<br>on which the instance of a Vivado Hardware Server is running. |        |  |  |  |  |
|              |  |        |  |  |  |  |
|              |  |        |  |  |  |  |
|              |  |        |  |  |  |  |
|              |  |        |  |  |  |  |
|              |  |        |  |  |  |  |
|              |  |        |  |  |  |  |
|              |  |        |  |  |  |  |
| E XILINX.    |  |        |  |  |  |  |
| ?            | < Back Next >  | Cancel |  |  |  |  |

8. In the Connect to field select Remote Server and in the Host name field enter your local machine's IP address.

| <u>C</u> onnect to:   | Remote ser  | rver (target is on remote machine) 🛛 🗸                                   |
|---|---|--|
| Remote Serv   | er  |  |
| <u>H</u> ost name   |   | S 🗸  |
| <u>P</u> ort:   | 3121  | [default is 3121]  |
| 9.Now Click on Progra<br>HARDWARE MANAGER - localhosth                                    | am Device in the l<br>xilinx_tcf/Digilent/210183794       | e Hardware Manager window. Select the bit file and hit Program           |
| Hardware  |   | fourbit addacu   |
| Q   ₹   €   Ø   ►   ×<br>Program Device   | >   <b>I</b>   <b>¢</b>                                   | C:/Xilinx/projects/trial_project.srcs/sources_1/new/fourbit_adder.v      |
| Select a bitstream programming<br>select a debug probes file that co<br>programming file. | file and download it to your<br>presponds to the debug co | our hardware device. You can optionally cores contained in the bitstream |
| Bitstream file: C:/Xilinx/<br>Debug probes file:  | projects/trial_project.runs/i                             | s/impl_1/fourbit_adder.bit   |
| ✓ Enable end of startup che   | ck  | Program Cancel   |

You can try a simple calculator example from <u>https://github.com/Digilent/Basys-3-Abacus</u>