CSE 490/590 Summer 2025 **Quiz 1 Solution**

[Question 1]
Suppose that we want to enhance the processor used for Web serving. The new processor is 6 times faster on computation in the Web serving application than the original processor. Assuming that the original processor is busy with computation 80% of the time, what is the overall speedup gained by incorporating the enhancement?

$$\text{Speedup}_{\text{overall}} = \frac{\text{Execution time}_{\text{old}}}{\text{Execution time}_{\text{new}}} = \frac{1}{(1 - \text{Fraction}_{\text{enhanced}}) + \frac{\text{Fraction}_{\text{enhanced}}}{\text{Speedup}_{\text{enhanced}}}}$$

Answer: $Speedup_{overall} = \frac{1}{(1-0.8)+\frac{0.8}{6}} = 3.0$

[Question 2]
Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. Which processor has the highest performance expressed in instructions per second? **Show your work** on the paper submitted.

Answer:
CPI = # clock cycles / # instructions
Clock rate = # clock cycles / # seconds
Performance =
Clock rate / CPI =
(# clock cycles / # seconds) / (# clock cycles / # instructions) =
(# clock cycles / # seconds) / (# clock cycles / # instructions) =
instructions / # seconds
Thus:
P1 performance = 3×10^9 / 1.5 = 2×10^9
P2 performance = 2.5×10^9 / 1 = 2.5×10^9 (highest performance)
P3 performance = 4×10^9 / 2.2 = 1.81×10^9

[Question 3]
Convert the following MIPS assembly instruction to its binary format:
addi $t0, $s0, 11

Answer: Using the MIPS Green Sheet
Opcode: 001000
rs: 10000
rt: 01000
Immediate: 001000 10000 01000 0000000000001011

[Question 4]
A program's runtime is determined by the product of instructions per program, cycles per instruction, and clock frequency. Assume the following instruction mix for a MIPS-like instruction set on the right, Compute the overall CPI:

Instruction Type	% of Instructions	Cycles
Store and Load	20%	4
Branch	10%	3
Integer ALU	30%	2
Shift	40%	2

Answer:
Overall CPI = (0.20*4)+(0.10*3)+(0.30*2)+(0.40*2) = 2.5
Explanation: The calculation performed is a weighted average of each of the individual types of the instructions that are present. In this question we assume that the CPU is a single cycle processor, thus each instruction will execute one after the other with no overlap. Each instruction takes a different number of cycles to fully execute.

[Question 5]
Consider a byte-addressable memory system with the following contents:

Memory Location	Value
0x8132	0x73
0x8133	0x49
0x8134	0x50
0x8135	0x76
0x8136	0x21
0x8137	0x93
0x8138	0x83
0x8139	0x13

CSE 490/590 Summer 2025 **Quiz 1 Solution**

If the following instruction is executed:
lw $t3, 2($t4)
$t4 contains the address 0x8132. What will $t3 contain? Use Big-Endian.
(e.g. if answer = 0x12345678, type in 12345678)

Answer:
$t3 contains 0x50762193

[Question 6]
Consider a byte-addressable memory system with the following contents:

Memory Location	Value
0x7FF2	0x02
0x7FF3	0x56
0x7FF4	0xA2
0x7FF5	0x4B
0x7FF6	0xF2
0x7FF7	0x92
0x7FF8	0x24

0x7FF9	0x35

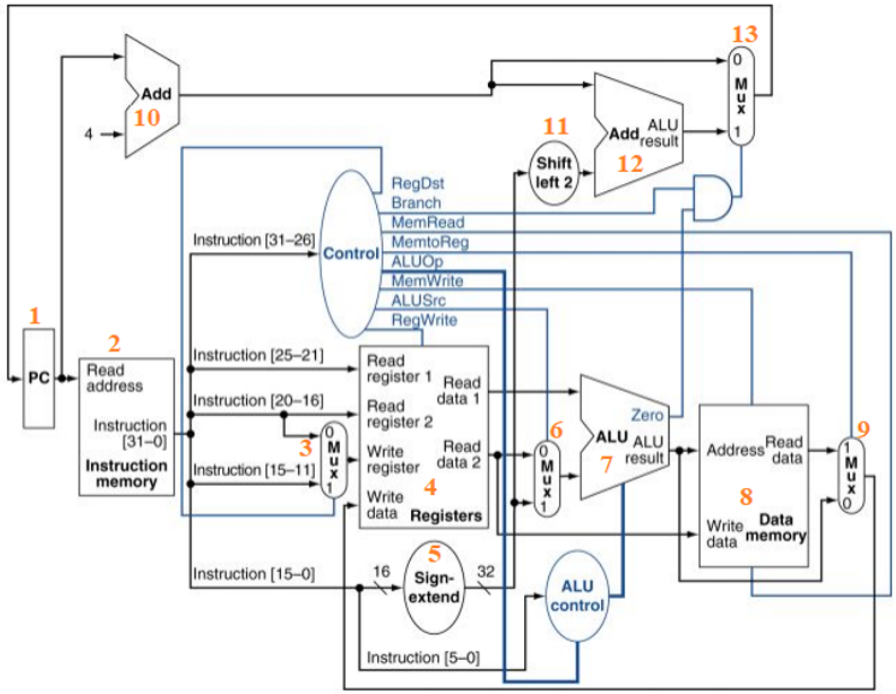
If the following instruction is executed:
lh $t3, 4($t4)

$t4 contains the address 0x7FF0. What will $t3 contain? Use Big-Endian.

Answer: $t3 contains: **0xFFFFA24B**
The lh instruction sign-extends the halfword (16 bits) into a 32-bit value. That is, the most significant bit of the 16-bit halfword is copied into the upper 16 bits of the register.
For example, if the loaded halfword is 0x89AB = 0b1000100110101011, the MSB is 1, so the sign-extended value will be 0xFFFF89AB (in 32-bit representation)

[Question 7]
Given below is the datapath of a single-cycle non-pipelined MIPS processor. Which components are required for executing the instruction SW (Store Word)? Check all that apply.

CSE 490/590 Summer 2025 **Quiz 1 Solution**



SW: 1,2,4,5,6,7,8,10,13

[Question 8]

Consider the following instructions and assume a MIPS 5-stage pipelined datapath (IF, ID, EX, MEM, WB):

sub $t2, $t3, $t4

lw $t5, 4($t2)

or $s1, $s2, $s3

sw $t7, 8($t5)

a. For the above instruction sequence list the data hazards. Explain your reasoning.

b. For the above instruction sequence, use data forwarding to overcome the data hazards and compute the total number of cycles needed. **Draw arrows to show forwarding.**

CSE 490/590 Summer 2025 **Quiz 1 Solution**

(Submit written answers after the quiz for grading. Alternatively, you can use the editor to create the table below to show the stages.)

Inst.	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
sub									
lw									
or									
sw									

Answer:

a. There are two data hazards:

- The 1st and 2nd instruction (sub and lw; t2 register is not updated soon enough for when the 2nd instruction will execute)
- The 2nd and 4th instruction (lw and sw; t5 register is not updated soon enough for when then 2nd instruction will execute)

Inst.	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
sub	IF	ID	EX	MEM	WB				
lw		IF	ID	EX	MEM	WB			

CSE 490/590 Summer 2025 **Quiz 1 Solution**

or			IF	ID	EX	MEM	WB		
sw				IF	ID	EX	MEM	WB	

The total number of cycles needed: 8 cycles