Conversion of Schematic to Layout

Step by step procedure to convert Layout to Schematic:

Part I: (opening Virtuoso XL)

1. Design the circuit in virtuoso schematic editor

2. Check and save the circuit

3. In Schematic Composer Window, Click on **Tools-> Design Synthesis -> Layout XL**

4. A dialog box appears asking if we were to open it in existing cell view, or new cell view. **Choose CreateNew** and click **OK**

5. The New File dialog box appears containing the name of the cell view, layout etc. Click **OK**

6. The layout editor opens.

Part II: (Generating Layout from schematic)

1. Click **Design-> Gen from source** in Virtuoso XL Window.

2. Layout generation options window appears. Do necessary modifications.
Example: The window will contain details of all the pins/nets used in the schematic. Input pins, Ground, Vdd, outputs pins etc must be metal layers. **It must be ensured that layer for these pins are chosen as metals**.

3. Click **Ok**. Press "**Shift + F**" to see the contents of the instances.

4. Click on **Edit -> Place As in Schematic** to place the instances exactly as placed in schematic.

5. You may place the components by using **Edit->Move** to achieve compactness.

Part III: (**What is what**)

Clicking the components in Virtuoso XL window will highlight the corresponding component from the schematic composer. By this, you can identify which component refers to which component.

or

Click on **Connectivity-> XL Probe.** All the pins in the circuit will appear. You may click any one of them to see where it is exactly placed in the layout window.

Part III: (**Connecting netlists**)

If you can infer, only the components and the pins are converted from the schematic window to Virtuoso XL. Hence we must give wirings between inputs and other netlists.

1. Viewing Incomplete netlists:
    a. Click **Connectivity-> Show incomplete nets.**
    b. Click either 'Select all' and 'OK' to view all the incomplete netlists
    or
    Click on 'any particular pin' to view the incomplete nets from that pin

    c. Click **Connectivity-> Hide incomplete nets.**

2. Use LSW (Layer Select Window) to **choose appropriate layer**. Either use '**Create Rectangle**' or **'Create Path'** to give a connection between pins and instances.

3. Remember to give a "**Contact**" of type "m1_m2", "m1_poly" etc. when required

Part IV: (**DRC**)

1. Do the Design Rule Checker for the layout.

2. If there are no errors, Extract the layout by setting appropriate switches.

3. Go to the extracted window and do the post layout simulation using specters.

4. Part IV is the same as what you did in Homework1. You can refer the course website for further details.