STABILITY ANAYSIS OF CMOS BASED SUBTHRESHOLD SRAM CIRCUITS

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***Abstract*— With the current trend in designing circuits that have low power operation characteristics, the focus is slowly shifting from size reduction to Low power consumption. From the semiconductor industry perspective, we have reached a point where shrinking the device size or packing a few more million transistors in a given space has reached a moot point. Only if a way to minimize the alarming increase in power consumption is satisfied, can we think of the next step in semiconductor process evolution. One such way is supply voltage scaling but having said that, we have a slew of problems that come with this innovation. This paper deals with the concept of sub-threshold operation and how this can be effectively utilized in memory circuits to improve the read/write stability even after operating them below the threshold voltage. The first part of this paper shows how an adaptive body biasing technique can be used to vary the threshold voltage. Rather than generally going ahead with the body biasing, this process is dependent on the operating frequency. The second part of this paper discusses on utilizing various subthreshold SRAM circuits and finding the optimum design in terms of reliability. This is done with the help of N stability curves. The whole project has been implemented in 45nm technology and the ensuing results are tabulated and analysed.**

***Index Terms*—Sub-threshold conduction, Adaptive Body Biasing, Ring Oscillator, SRAM, Schmitt trigger, N Stability curves, SVNM, SINM, Monte Carlo Simulation.**

I. INTRODUCTION

Subthreshold circuits have gained immense usage in wireless sensors and biomedical applications mainly due to their low Power consumption characteristics. Unfortunately, Disadvantages such as increase in leakage current, performance issues and high sensitivity to noise have confined the usage of this domain to low performance spheres. Before moving forward with the project work, some of the earlier works in this field have to be mentioned. Authors in [1] have explained in the detail the need for operation in subthreshold region, its possible advantages and disadvantages. Moreover, some ways to negate the shortcoming though not altogether have also been given. The next paper listed as [2] gives a good idea about how the concept of adaptive body biasing can be employed to gradually scale down the threshold voltage, thus aiding in the operation in subthreshold region. The paper [3] was highly useful in explaining the concept of varying the body biasing as a function of operating frequency. Though the main concept of using Ring Oscillator as a part of adaptive body biasing is found in much detail in [4], the authors of [3] were very accurate in using this concept with the correct peripheral circuits to achieve the biasing as a function of the operating frequency. The paper [5] details on the possible SRAM circuitry and the reasons why most of them are not suitable for subthreshold operation. The same authors have proceeded to discuss in detail about Schmitt trigger based circuitry in [6] and [7] and how these can be used effectively as a subthreshold SRAM design technique. The proposed design to overcome the disadvantages of the Schmitt trigger based designs in the above mentioned papers has been used from the paper mentioned in [8]. To model the stability for all these circuits, the basics

of SRAM stability was refereed to from paper [9]. A few more papers listed as [10], [11] and [12] deals with the same topic but provides a more clear understanding of how to perform stability analysis with a SRAM circuit. The Monte Carlo simulation for this project implemented using Cadence virtuoso was performed as per the Iowa state Wiki entry in the link [13]. Low power designs need proper proof of reliability to show their validity in comparison to other existing circuits. Thus this paper starts with discussing the problems and the usefulness of subthreshold operation and finally end in proposing circuits to prove the reliability claim. Section 3 discusses the adaptive body biasing technique and the components involved in it in depth. Section 4 discusses the SRAM design techniques and analyses the advantages and disadvantages of each of the designs mentioned. Section 5 discusses the results by comparison with the existing SRAM techniques and shows quantitative proof of increase in reliability. Section 6 discusses future works that can be done with these design techniques and the scope for improving reliability using even further changes to the process and thereby concluding the paper.

II. SUBTHRESHOLD CHALLENGES

Some of the main problems associated with subthreshold operations is their susceptibility to external noise. This is due to the fact that in the subthreshold region, the ration of ON current to the ratio of OFF current that usually is about 10^8 reduces to near thousands. The physical Implications of this being that the ON current in subthreshold ranges in the domain of noise. And the OFF current also is in the same range. This causes the circuit to be most likely be turned on by rampant noise signals. Another main problem in this mode is the fact that as the supply voltage reduces, the leakage current increases. This causes the entire power consumption of the circuit to be based on the leakage power. The equation to calculate the total power for a circuit is given as follows:

$$E_{total} = E_{dynamic} + E_{static} = C*Vdd2f + IleakVddTtask \quad (1)$$

This proves that as the supply voltage reduces, the leakage power starts to dominate and this results in a huge problem, Further there is the additional concern of increased delay when operated in subthreshold region. These are shown graphically as below:

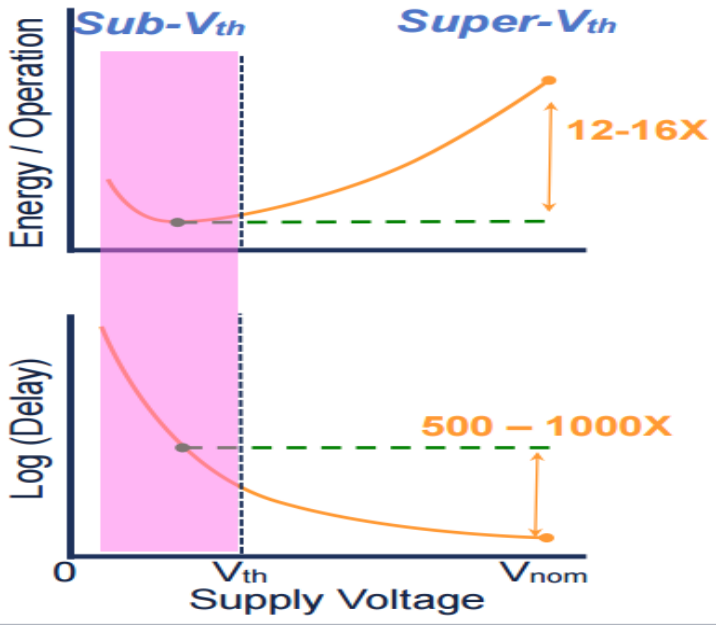


Fig1. Variation of Energy and delay in subthreshold region of operation

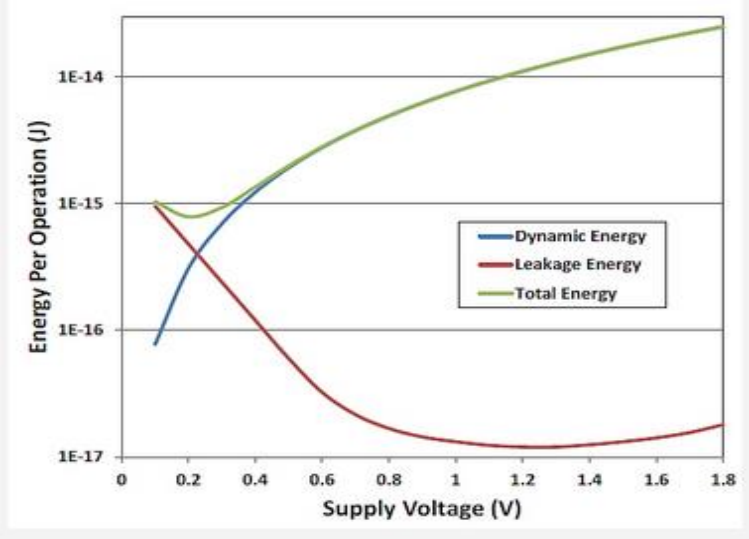


Fig 2. Graph showing dominance of leakage power in subthreshold region in accordance with the above mentioned equation (1)

As discussed the ratio of Ion to Ioff would be greatly reduced when operated in subthreshold region. This serves as the basis to explain the huge issue of leakage that we face. Having discussed all the issues, we fail to recognize the boon of this method. It is to be noted that even if leakage power is high, the overall power greatly reduces thus helping in operating the circuit in Ultra low power region of operation. This provides one of the main reasons to applications preferring subthreshold region of operation.

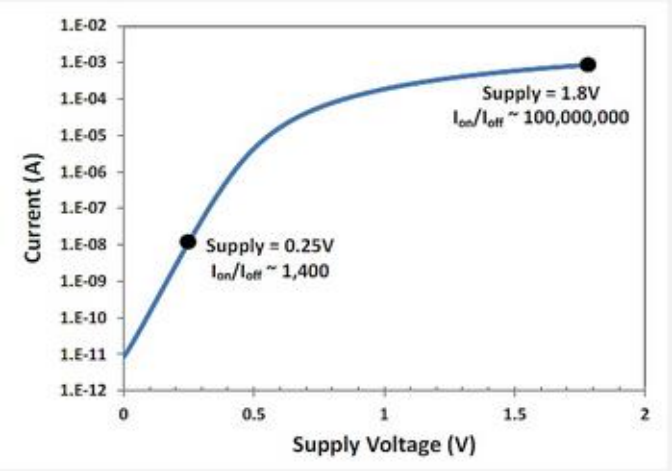


Fig 3. Ratio of On current to Off current in super threshold and sub threshold region.

III. ADAPTIVE BODY BIASING USING RING OSCILLATOR

A forward biased MOSFET can be operated in lower volatges or higher operating frequencies based on the following equation:

$$V_{T,N} = V_{T,N0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

Where Vt,N0 is the zero bias threshold voltage, Vsb is the source to substrate voltage, gamma being the body effect coefficient and phi being the Fermi potential.

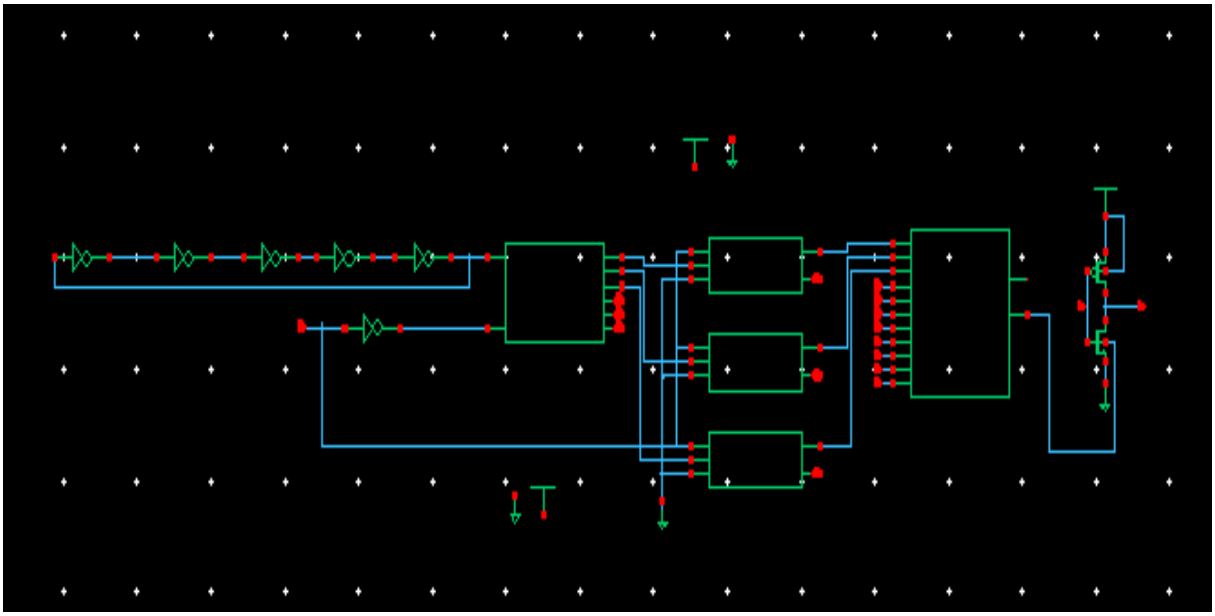


Fig 4. The adaptive body bias generator circuit.

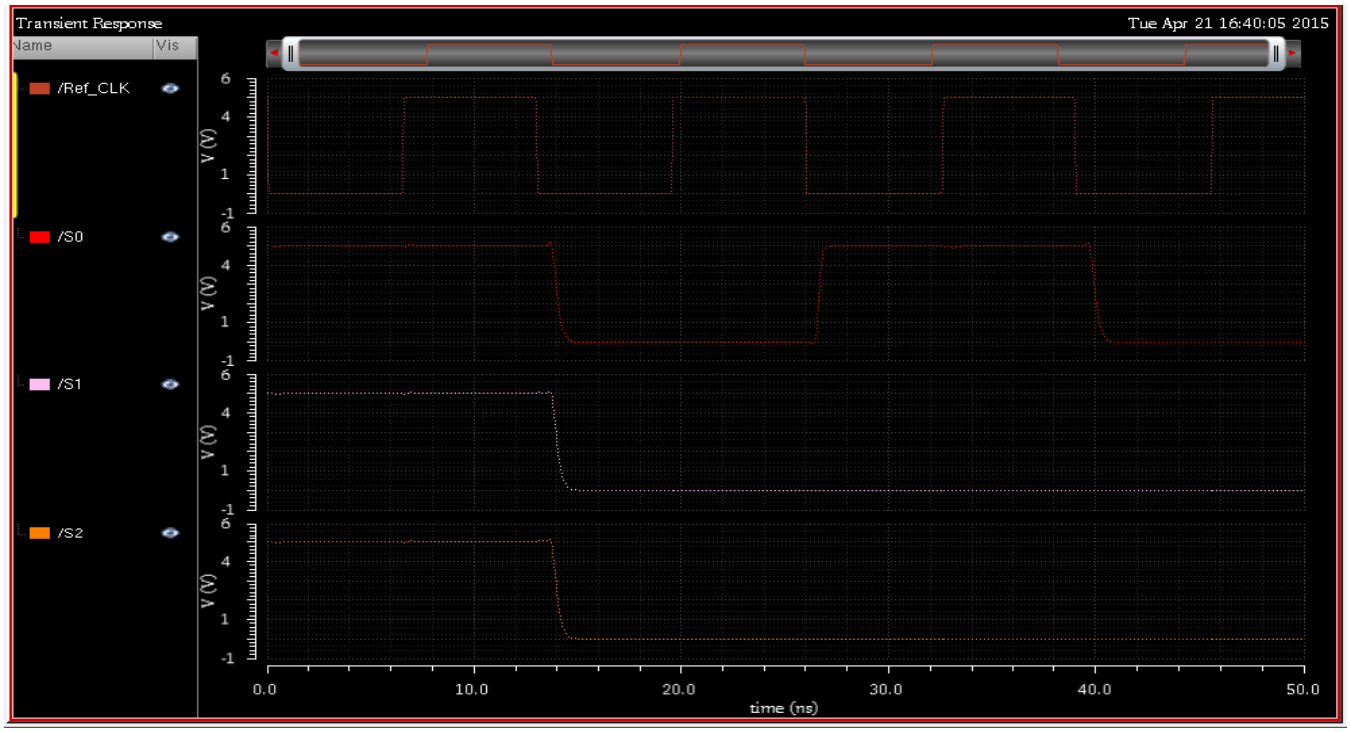
The above figure shows the adaptive body bias generation method using ring oscillator. The basic circuitry consists of a ring oscillator, 3 bit up counter, D flip flops and a 8:1 MUX. The ring oscillator has odd number of inverters to generate out of phase signals as compared to the input. This generates a continuous clock pulse whose frequency can be varied. This is done by varying the propagation delay of the inverter circuit. This and the reference clock of the circuit is fed as input to the 3 bit counter. The output of the ring oscillator starts the counter. As it is a 3 bit counter, the counting takes place from 000 till 111. The value of the counter is reset when the clock pulse of the reference clock goes high. Thus starting of high phase in the ref clock stops the counting and the 3 bit output is then given to the D flip flop which is activated by the clock input from the reference signal. The output of the 3 flip flops are then passed on as selection lines to a 8:1 MUX. Thus the counter value selects the bias to be provided. This is as follows:

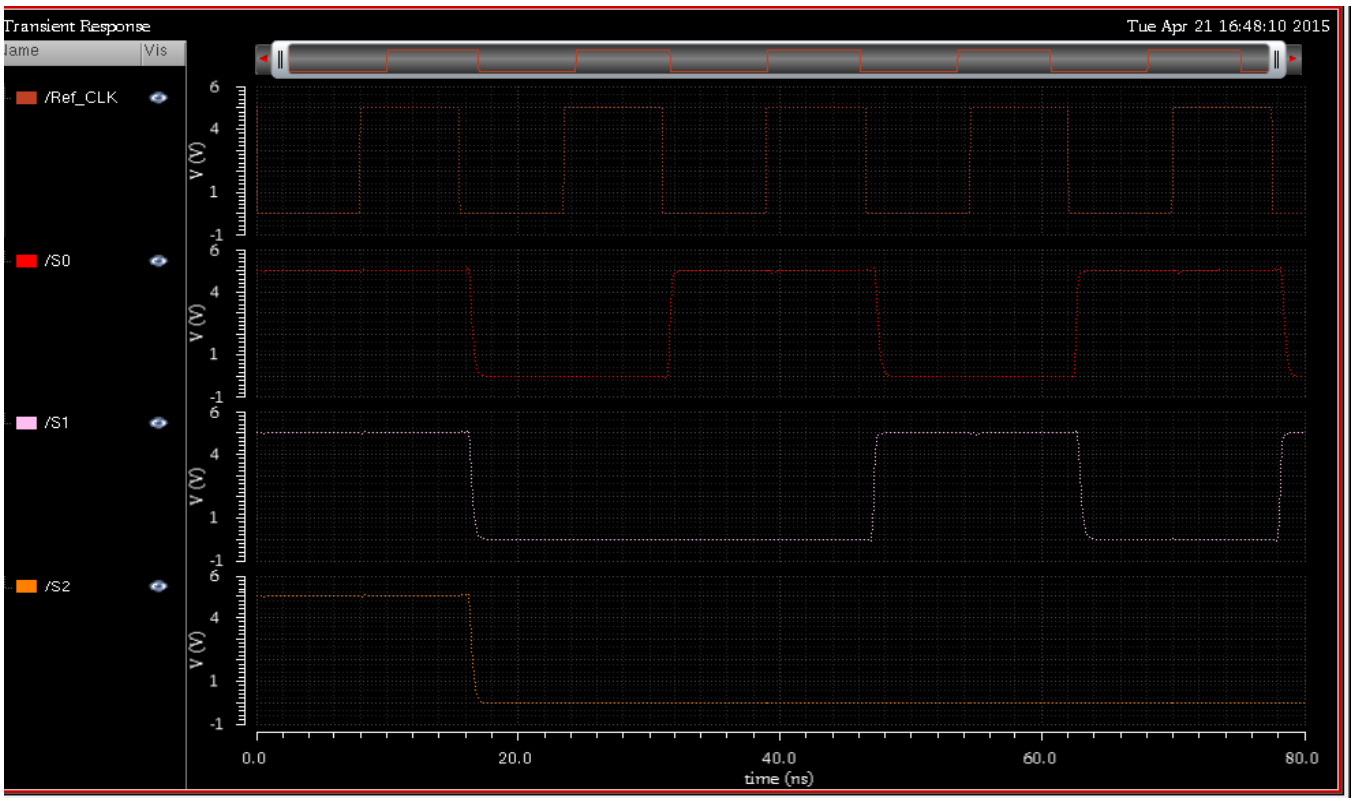
Output of 3-bit D flip flop	Output of multiplexer V_{bias}	V_{bias}
000	$V_{bias,0}$	0.3V
001	$V_{bias,1}$	0.2V
010	$V_{bias,2}$	0.1V
011	$V_{bias,3}$	0V
100	$V_{bias,4}$	−0.1V
101	$V_{bias,5}$	−0.2V
110	$V_{bias,6}$	−0.3V
111	$V_{bias,7}$	−0.4 V

Fig 5. Variation of bias voltage as per the counter value

The input to the MUX are the 8 bias values ranging from 0.3V to -0.4V. Thus based on the selection input from the counter, the appropriate value of the biasing is provided to the circuit. As all the values here are below threshold voltages themselves, a normal 8:1 CMOS gate based MUX cannot be used. Thus a transmission gate based MUX have to be utilized for this purpose.

The output obtained in Cadence as the reference clock is varied for various values are as follows:





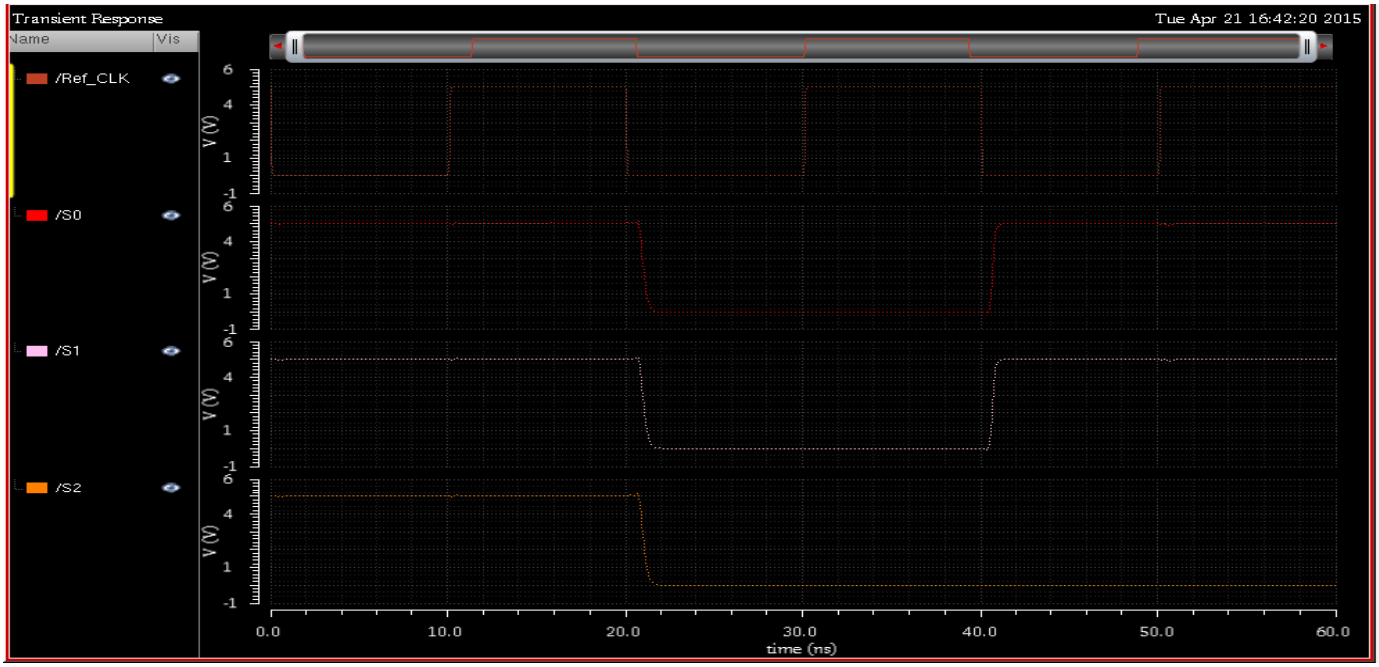


Fig 6. The variation of the counter value for 3 time periods (13ns, 15.5ns, 20n) of the reference clock.

This has been carried out for the first 4 frequencies and their variation of the bias voltage has been graphically represented as follows.

Frequency(MHz)	Time Period (ns)	Vbias (V)
100	10	0.3
74.07	13.5	0.2
64.51	15.5	0.1
50	20	0

Table 1: Variation of operating frequency with Biasing

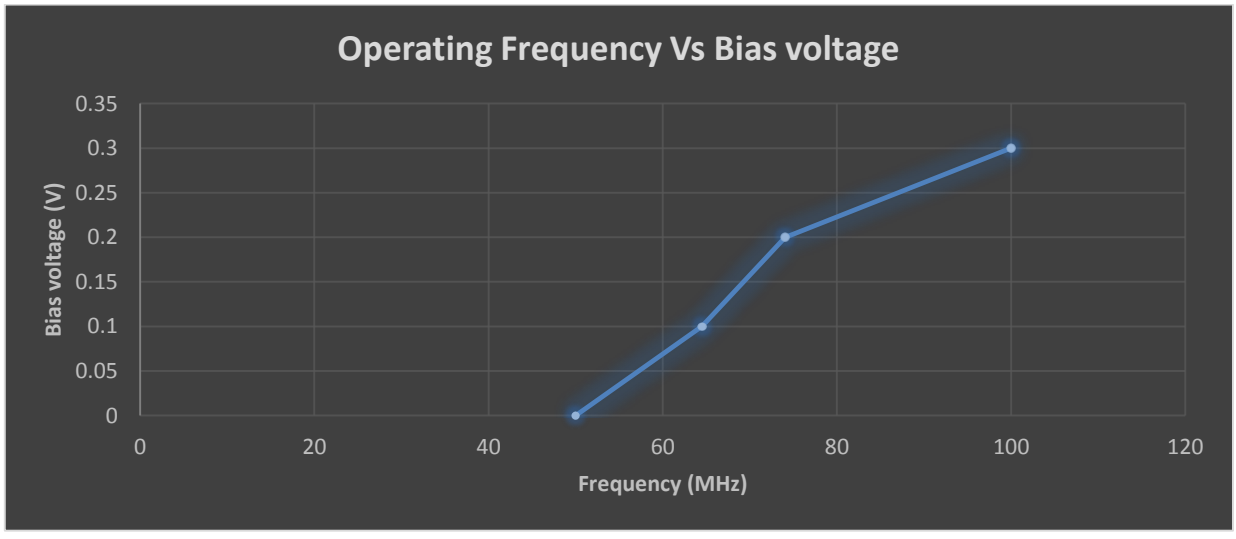


Fig 7. Variation of Bias voltage with frequency

IV. SUBTHRESHOLD SRAM DESIGNS

In the SRAM design to be discussed henceforth, as dimensions keep scaling down to nm scale, the variations in Vth and the stability factors play a major role in its performance. As discussed in [5], there are various SRAM designs namely single ended, differential, bit interleaving, Schmitt trigger based, virtual ground and DCVSL based techniques. To analyze the stability of the SRAM for sub threshold operation, we are currently interested in comparing the basic 6T, Schmitt trigger -1 and -2 as mentioned in [6] and [7]. The stability of all these circuits are recorded using the N stability curves. The reason for going in for N curves rather than just directly proceeding for SNM comparison is due to the fact that, we can have 2 circuits with the same SVNM and SINM values but that does not mean that they both have the same stability. Thus we need a combination of SNM value obtained from the butterfly curve as well as the N curve based values to correctly notice the
stability of the circuit. Here we use 2 factors namely SVNM and SINM. SVNM refers to static voltage noise margin. This is the maximum tolerable DC noise voltage before the content in the memory changes. SINM is Static Current noise margin that represents the maximum tolerable DC current over which the content inside the circuit changes. SVNM is calculated by taking the difference of the voltages where the stability curve crosses 0. The peak current in between these two provide us with the SINM. The values are obtained for all the designs and finally compared in the form of graphs.

A. SIMPLE 6T SRAM

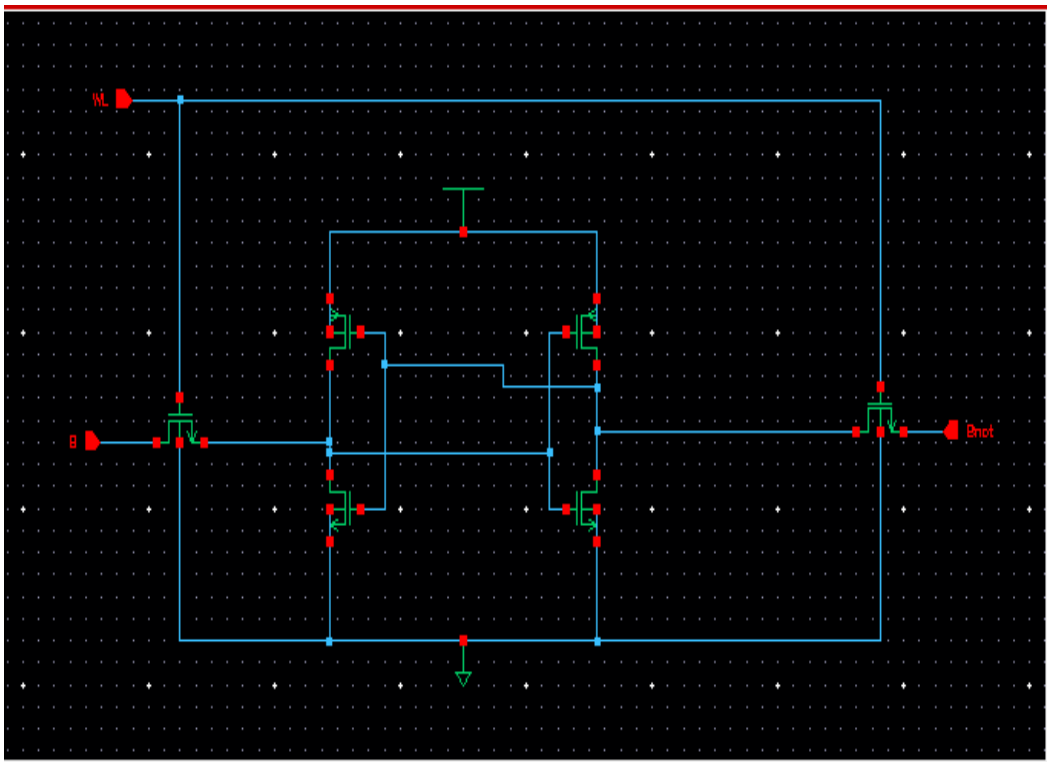


Fig8. Simple 6 transistor SRAM

The operation of this SRAM is as follows. The 6T SRAM consists of a pair of cross coupled inverter connected to bit-lines
(B and Bnot) through 2 access transistors. these are NMOS transistor. To start writing, we pass '1' to the WL line. And for read, the WL line is left as 0.The data to be written inside the circuit is provided through the bit

lines B, bnot. Thus providing these inputs and enabling the WL signal will write the data into the circuit. As the cross-coupled inverter is a strong feedback circuit, it is not inherently susceptible to noise, but any noise which passes through the lines can easily flip the stored values.The main problem with this design is that there is a inherent confusion for flipping. As during read, it should flip but in write the value must flip. During the read operation, the '0' storing node voltage is perturbed which might flip the stored data. For reliable read operation, the design requirement is such that the data should not be flipped. This is mainly because we use the same pair of buses to read and write into the cell. If a separate Sense amplifier is not used then this may cause serious issues during read cycle. The circuit works properly with a specific device sizing but this cannot be implemented as we move to lower channel lengths ranging in few tens of nm. The N curve for the above circuit has been attached as well. The SVNM and the SINM has been found individually for supply voltages 1V, 0.5V, 0.3V, 0.2V and 0.1V. Hence a updated design is needed for proper low voltage operation.

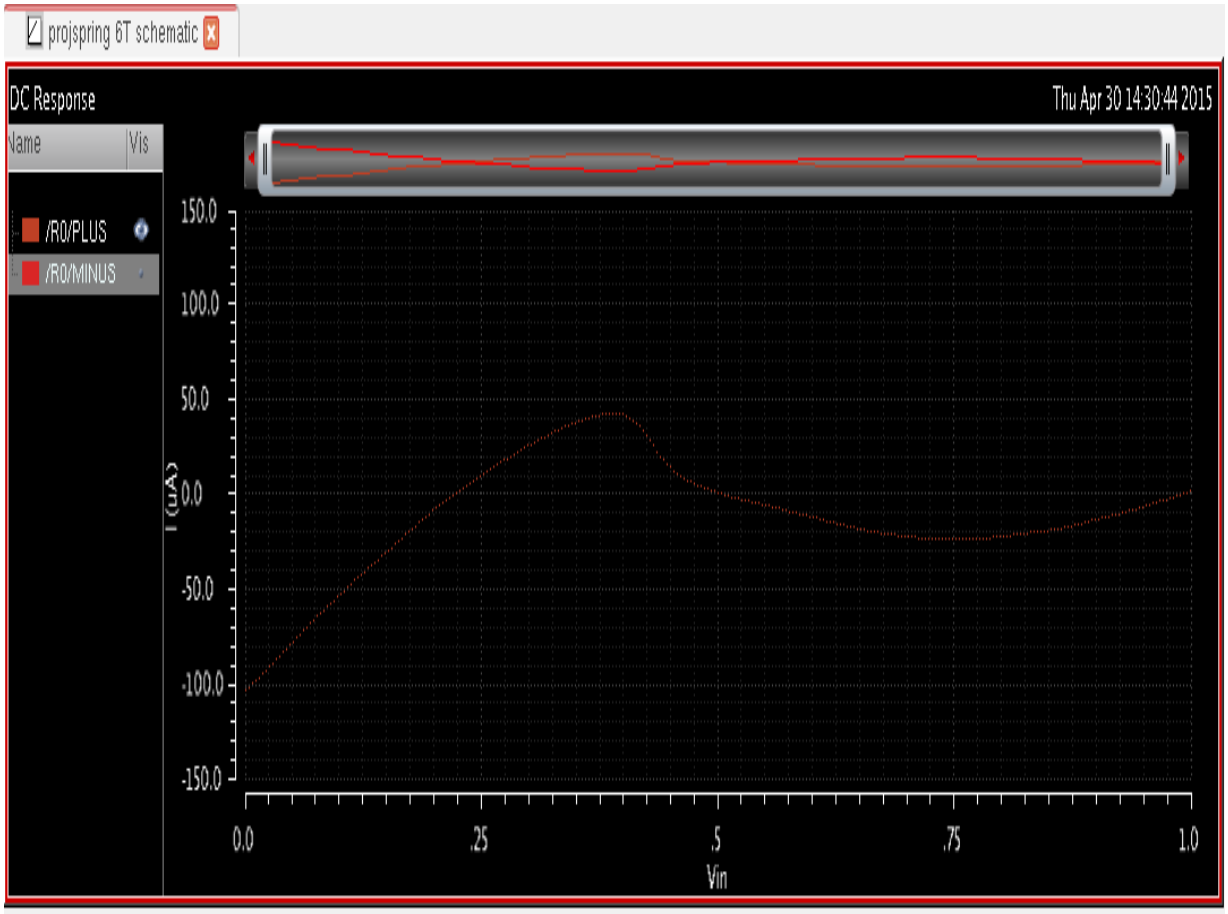


Fig 9. N curve for 6T SRAM at Vdd=1V.

Table 2. SVNM and SINM values for 6T SRAM at various supply voltages

Vdd (V)	Va (mV)	Vb(mV)	SVNM (mV)	SINM
1	223.6294	503.8864	280.257	42.2836u
0.5	74.34522	252.5551	178.2098	16.1294u
0.3	34.49116	154.9077	120.41764	1.219u
0.2	27.65984	103.66219	76.00235	96.00726n
0.1	36.66052	54.22165	17.56113	553.1p

B. SCHMITT TRIGGER BASED ST-SRAM

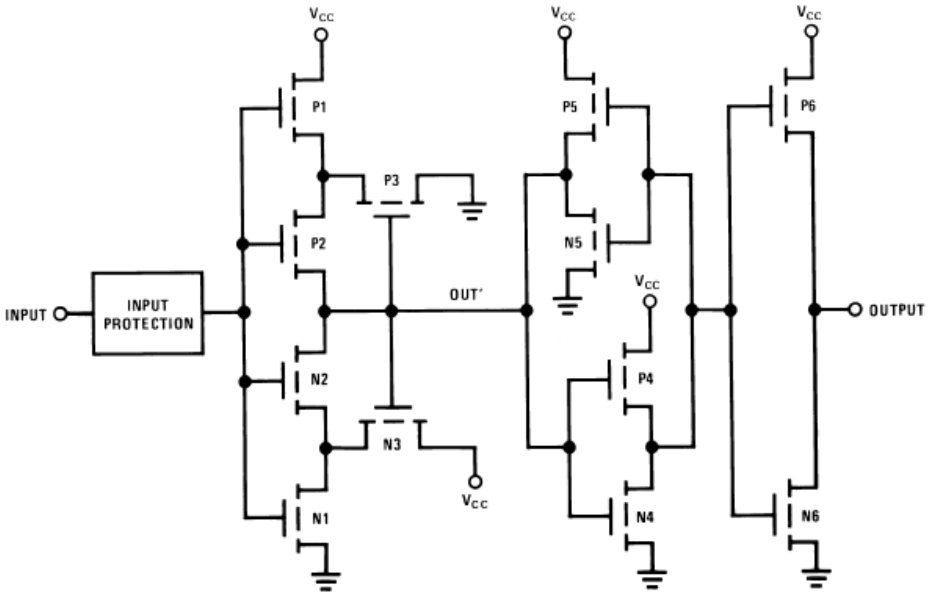


Fig10. CMOS based Schmitt trigger circuit.

The operation of a Schmitt trigger is as follows. Transistors P3 and N3 feedback the output voltage, out', to two different points in the circuit. When the input is given as 0V, transistors P1, P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON, the drain of N1, which is the source of N2, is at Vdd − VTH.As the input increases to Vth, N1 begins to turn ON, both N1 and N3 are ON thus forming a voltage divider network biasing the source of N2 at Vdd/2. When the input increases to vdd/2+vth, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' N3 stops supporting the voltage divider part with N1 , further lowering out'. Meanwhile P3 has started to turn ON due to decreasing out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to positive feedback of P3 transistor.

When the input is brought low again an identical process occurs
in the upper portion of the stack and the snapping action takes place when the lower threshold its reached. Out' is fed into the inverter formed by P4 and N4.
For the first Schmitt trigger circuit to be implemented, we don not use 2 feedback loops. For the 1 to 0 input transition the feedback mechanism is not present. This results in smooth transfer characteristics mainly for easy write operation. The main advantage of this is that the node storing 0 can be flipped only at high voltages. This dramatically increases the write ability in comparison to the 6T circuit.

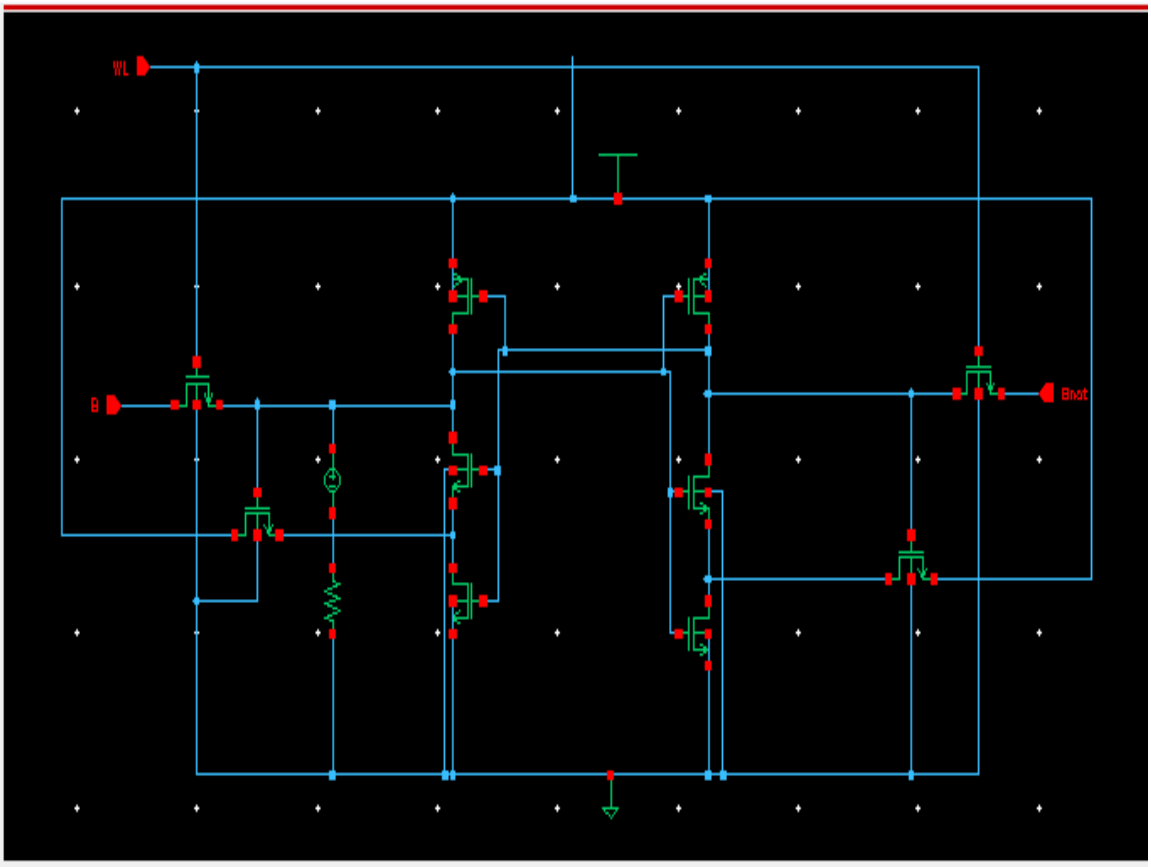


Fig 11. ST-1 based SRAM circuit.

A further improvement over the ST-1 SRAM circuit is the ST-2 SRAM design. The main difference is that there are 2 word-lines (WL/WWL).The WL signal is made high during the read as well as the write operation, while WWL signal is made high only during write operation. In ST-2 cell, feedback is provided by additional WL signal where, as in ST-1 cell, the feedback is provided by the internal storage node.

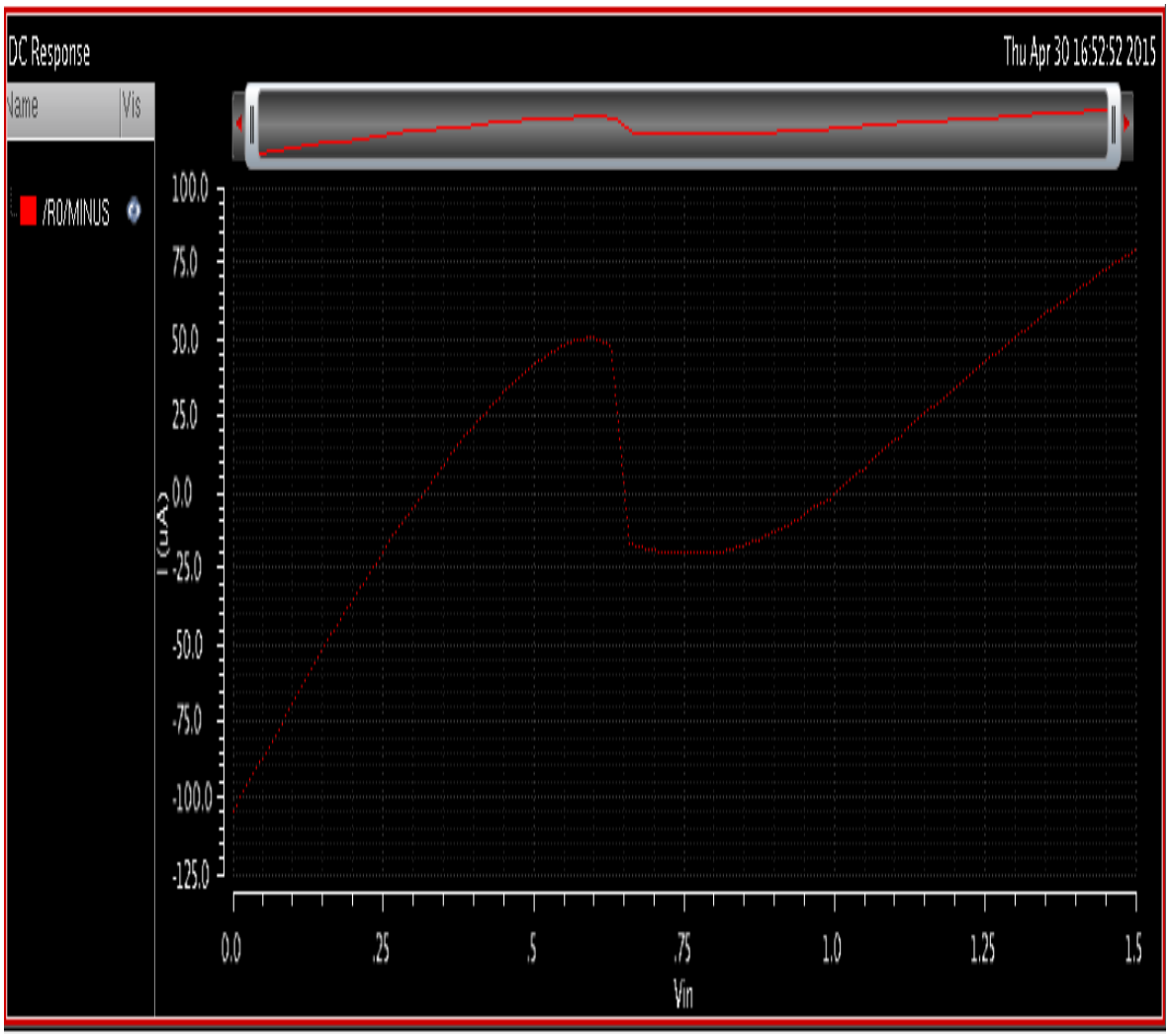


Fig 12. N curve of ST-2 SRAM circuit at Vdd=1V

Table 3. SVNM and SINM values for ST-2 circuit.

Vdd (V)	Va (mV)	Vb(mV)	SVNM (mV)	SINM
1	316.3518	652.0552	335.7034	50.616u
0.5	105.4035	326.2587	220.8552	10.3307u
0.3	52.2182	205.4168	153.1986	803.94n
0.2	42.3537	131.3378	88.9841	74.8153n
0.1	51.0065	80.09247	29.08597	836.6p

The operation for ST-2 circuit is as follows: During the read operation, let us assume that N2-N1(say x) junction is storing 0 and the P2-N2(say y) is storing 1.When WL is turned ON, (WWL is OFF during read) the voltage at x raises above 0. Since there is no current through WWL transistor,y is equal to the x. For the inverter storing '1', the feedback mechanism is provided by the WL access transistor .This results in incresased read stability compared to the 6T cell. Moreover, feedback NMOS can track pull down NMOS variations across the process corners giving improved process variation tolerance.

Mainly, the storage node is isolated from the read current path; it results in reduced capacitive coupling from the switching WL.

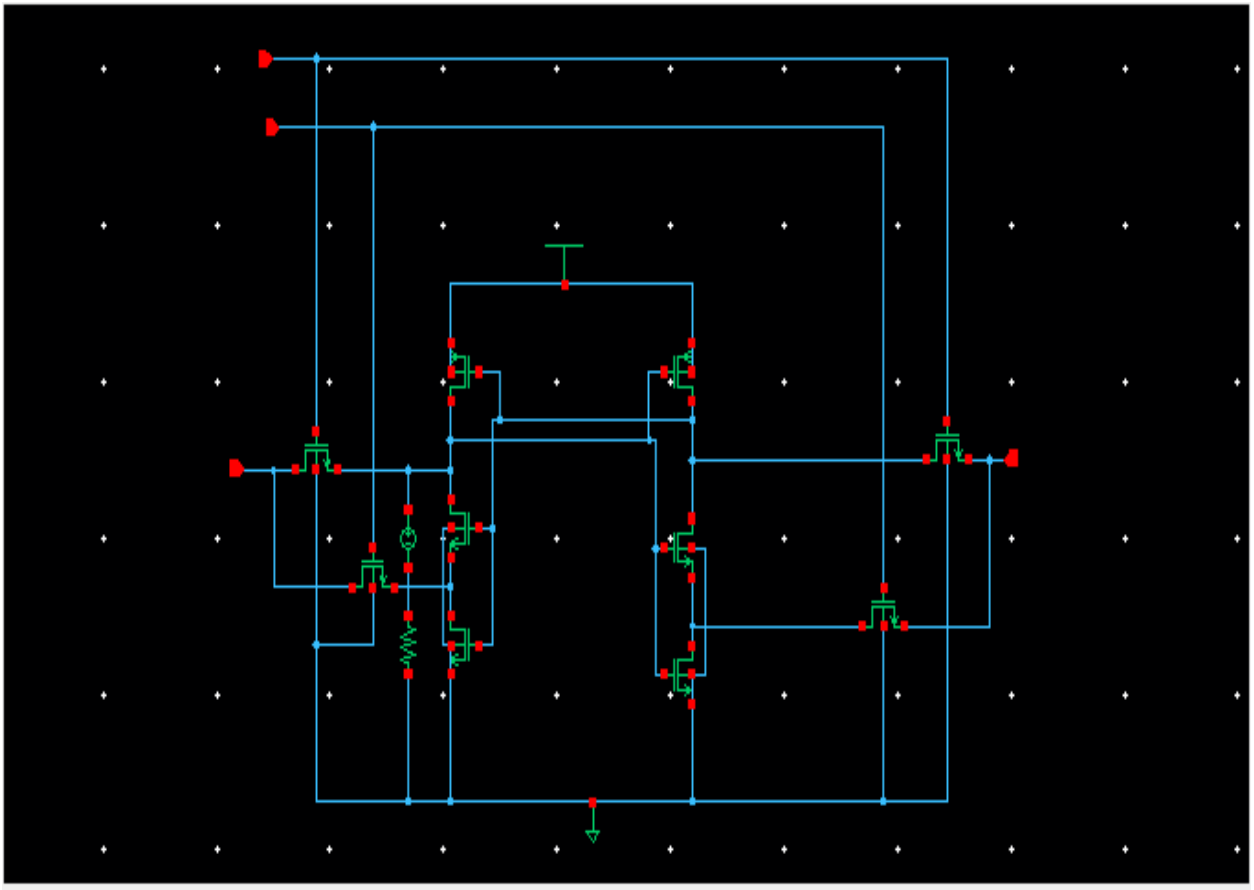


Fig 13. ST-2 ST-SRAM circuit

C. VIRTUAL GROUND ST-SRAM CIRCUIT

Even though the read stability of the schmitt trigger has been improved compared to the 6T cell, there exists a minor problem with this type of ST cell. It still suffers from the read disturbance problem, which refers to the phenomenon that a storage node with data '0' will experience a transient voltage glitch when it is being read. This voltage glitch may sometimes cause the cell to flip unexpectedly. To mitigate this issue, we have a virtual ground based circuit. The design of this cell is very similar to the Schmitt trigger-2 circuit, meaning it uses two

wordlines. One of them (denoted asWL) is for the read operation and the other (denoted as WWL) for the write operation. Each storage node (either Q or Qb) is now connected to a bitline by two cascaded access transistors, controlled by WL and WWL, respectively. Although this cell can have a better Read SNM (Read Static Noise Margin), its writeability is sacrificed due to the larger resistance between the bitline to the storage node, since the driving path is now formed by two access transistors connected in series. Another change here is that there exists one extra signal called VGND, denoting a virtual ground signal. This VGND signal

is connected to GND only during the read operation. Otherwise, it is connected to VDD. Here each of the cross-coupled inverters is composed of three transistors cascaded in a P-P-N sequence from top to bottom. The nodes between the two cascaded P-MOS transistors are called pseudo storage nodes apart from the real storage nodes. In addition to the inverter pair, there is a discharging path on each side of this SRAM cell, each of which is formed by an access transistor plus some pull-down transistor that connects a pseudo storage node to the VGND. In general, this new SRAM cell design offers several merits over the ST as well as 6T cells.Unlike the ST cell , there is no read disturbance problem at all, considering that the discharging path is now isolated from the true storage node. There might be some transient voltage glitch at the pseudo storage node during the read operation, but not the true storage nodes. Moreover, the true storage node is better grounded by the VGND

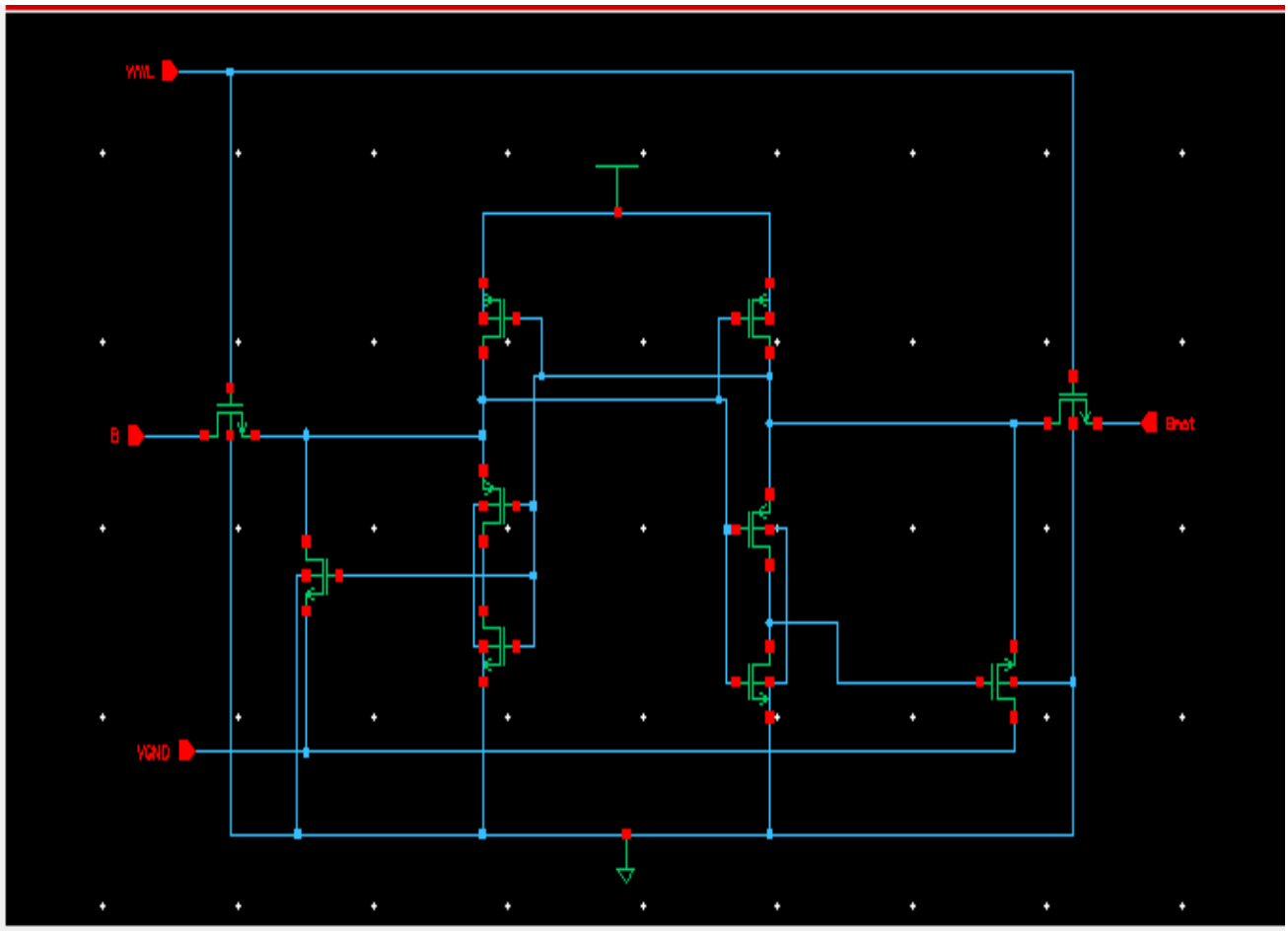


Fig 14. Virtual ground based PPN ST-SRAM

Vdd (V)	Va (mV)	Vb(mV)	SVNM (mV)	SINM
1	223.161	677.2279	454.0669	34.29u
0.5	75.4197	337.6704	262.2507	6.2293u
0.3	35.5449	199.3686	163.8237	493.94n
0.2	27.1857	134.3991	107.2134	51.145n
0.1	29.5832	69.4812	39.898	1.33015n

Table 4. SVNM and SINM values for VGND based PPN ST-SRAM.

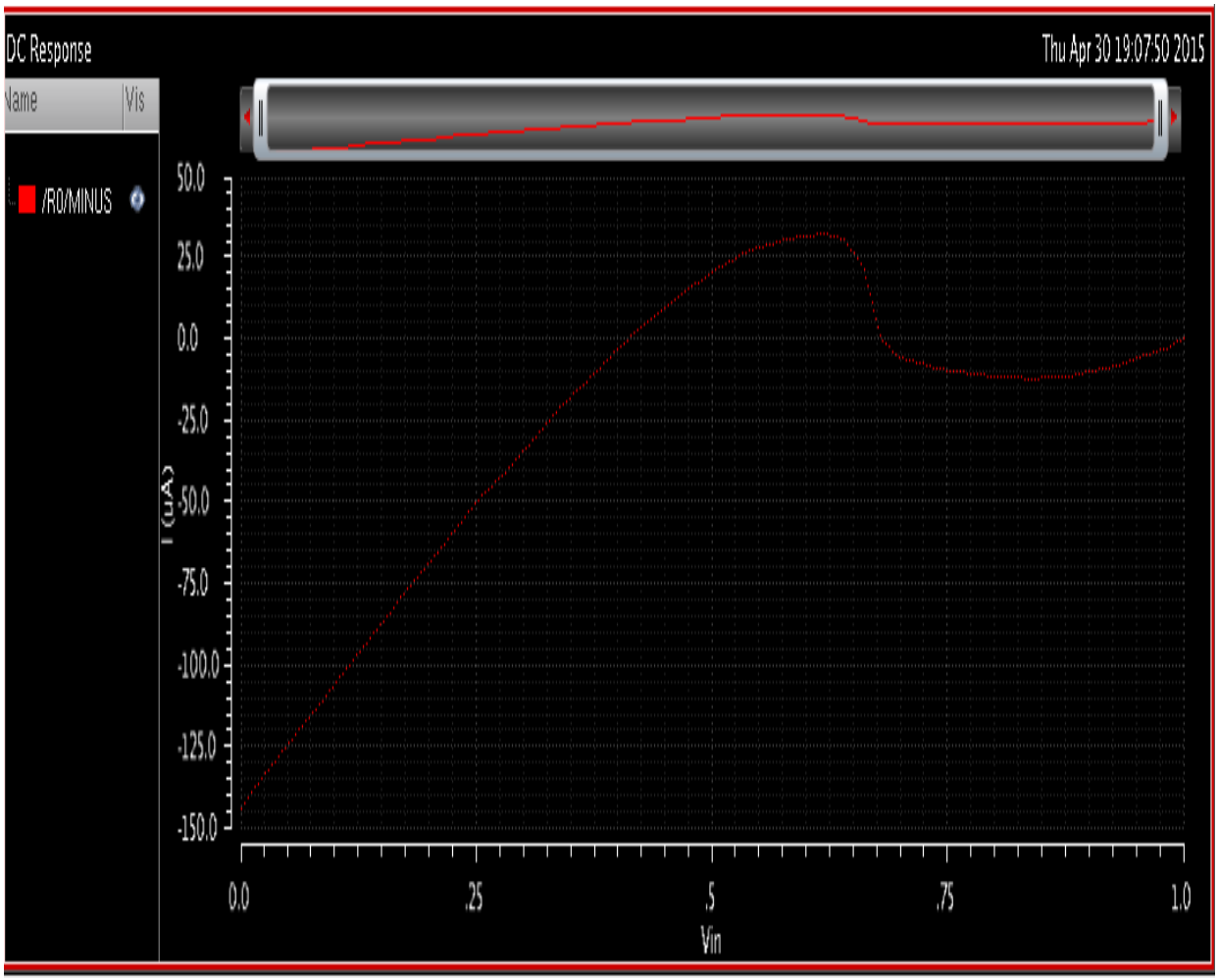


Fig 15. N stability curve at Vdd= 1V

V. ANALYSIS OF RESULTS

A comparison of the stability factors can be obtained now to estimate the optimum design suitable for subthreshold operation among the designs discussed so far.

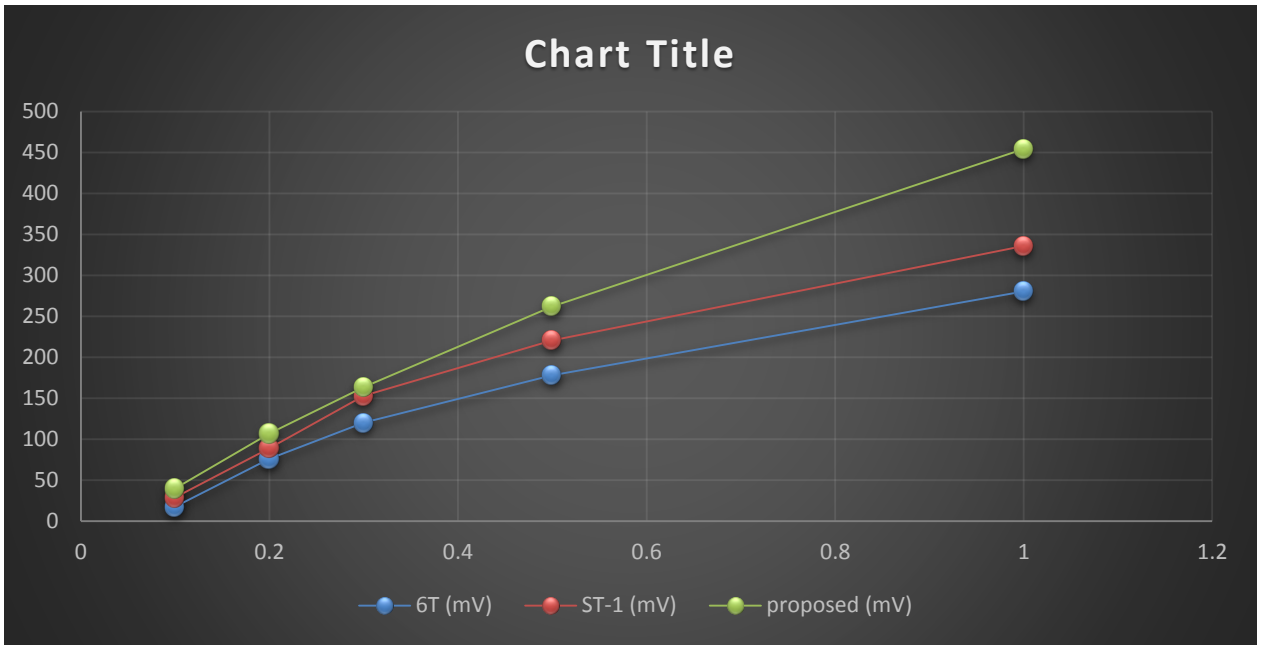


Fig16. Comparison of SVNM for 6T, ST-1 and VGND based PPN design.

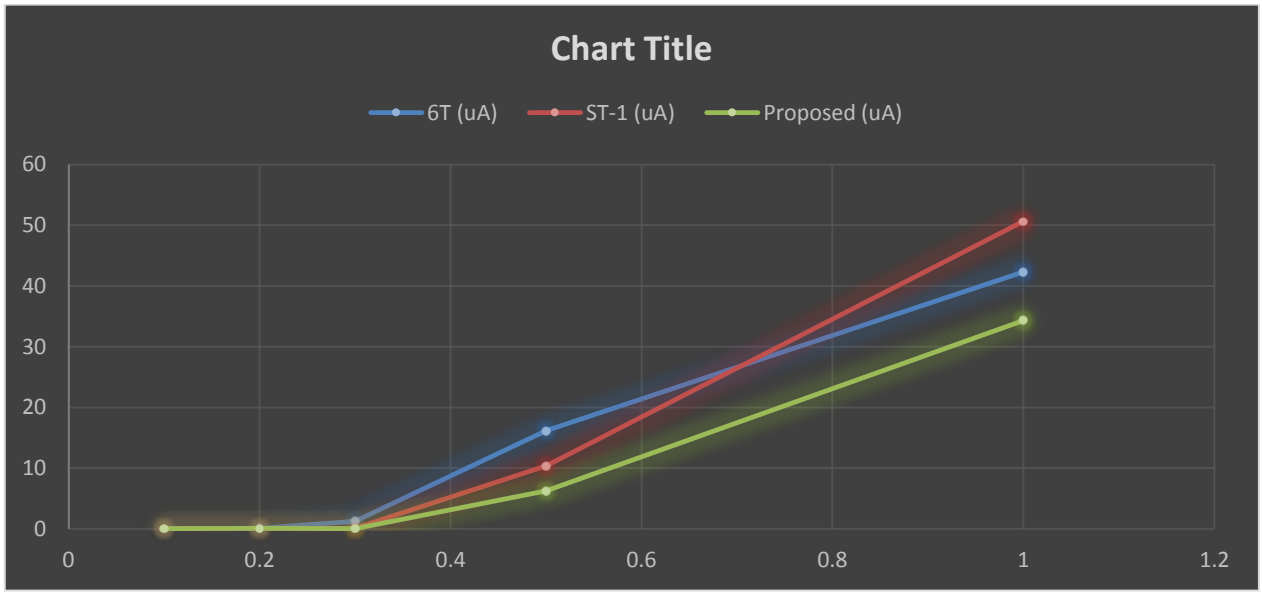


Fig 17. Comparison of SINM for 6T, ST-1 and VGND based PPN design.

Thus we are able to infer the following points. The SVNM of the proposed design is the highest of all three design proving that it can accept a range of DC voltages before the bit stored can change. This proves the increased write stability. Moreover, the SINM of the proposed design has the highest SINM value proving that the tolerance against leakage is comparatively higher at lower voltages.

VI. Future works and potential improvements

While it is apparent that there are new methods coming up every day that improves the read and write stability, this project has focused on 4 main designs. Thus more circuits such as Bit interleaving techniques [14][15], DCVSL[16] techniques are yet to be explored. A better way to map the increase in stability of each design is by using Monte Carlo Simulations to understand process variations such as temperature effect on Ion / Ioff value and the leakage current in each of the designs.

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