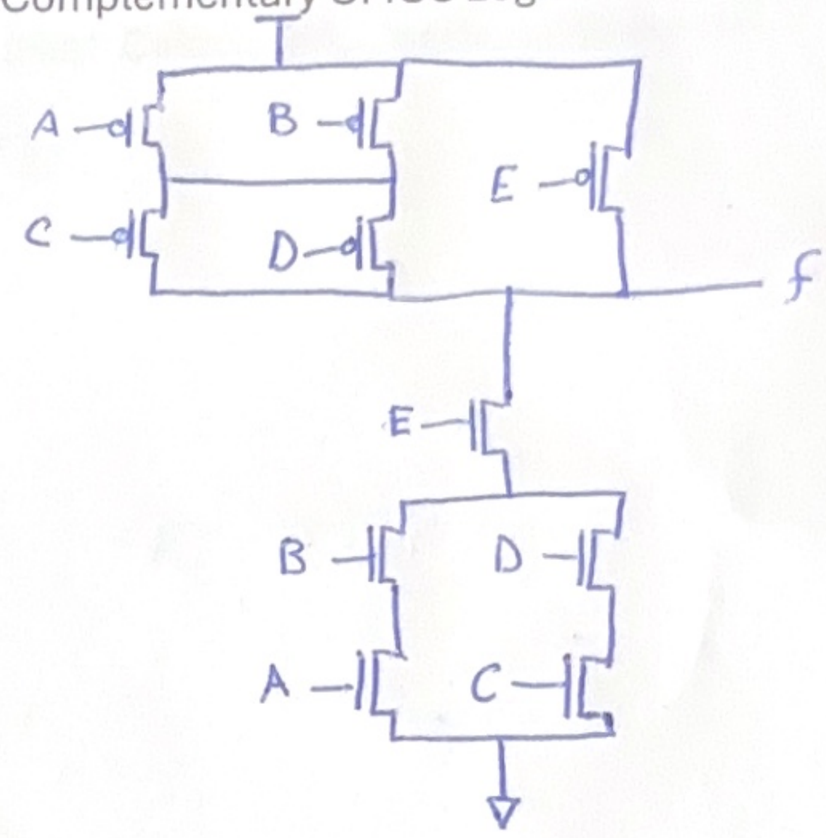
CSE 493/593 FALL 2025 QUIZ 1 - Duration: 50 minutes **50 points**

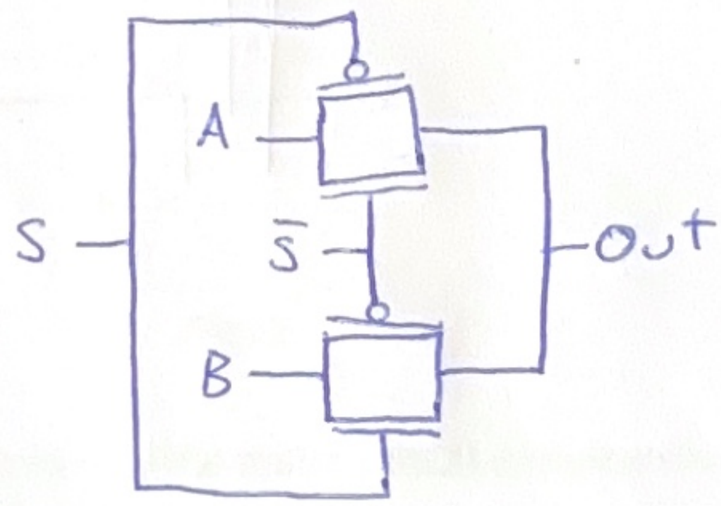
1. [10 pts] Implement the given logic function using Complementary CMOS Logic.

   $f = \wedge[((A.B+C.D).E)]$ =>PDN

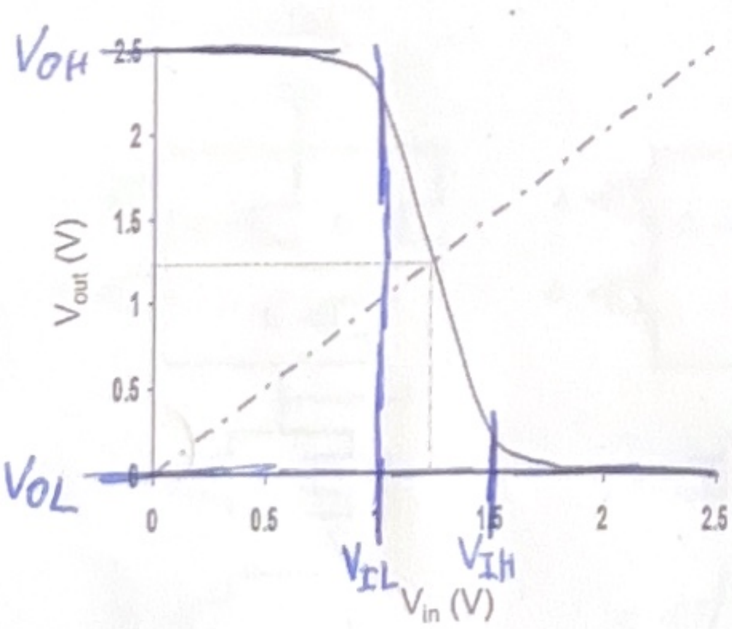
   $f = (\bar{A}+\bar{B})\cdot(\bar{C}+\bar{D})+\bar{E}$ =>PUN



2. (8 points) Design a 2:1 Multiplexer using CMOS Transmission Gate Logic. Consider inputs A, B; Select line: S; Output: Out



3. (10 points) Voltage Transfer Characteristics of an inverter is given in Fig 1. Determine V_{IL}, V_{OL}, V_{IH}, V_{OH} , N_{ML} and N_{MH}. Show the steps



$V_{IL} = 1V$

$V_{IH} = 1.5V$

$V_{OL} = 0V$

$V_{OH} = 2.5V$

$N_{ML} = V_{IL} - V_{OL} = 1V - 0V$

$N_{MH} = V_{OH} - V_{IH} = 2.5V - 1.5V$

Fig. 1

4. (10 points) Input and output waveforms of a CMOS inverter are given in Fig. 2.

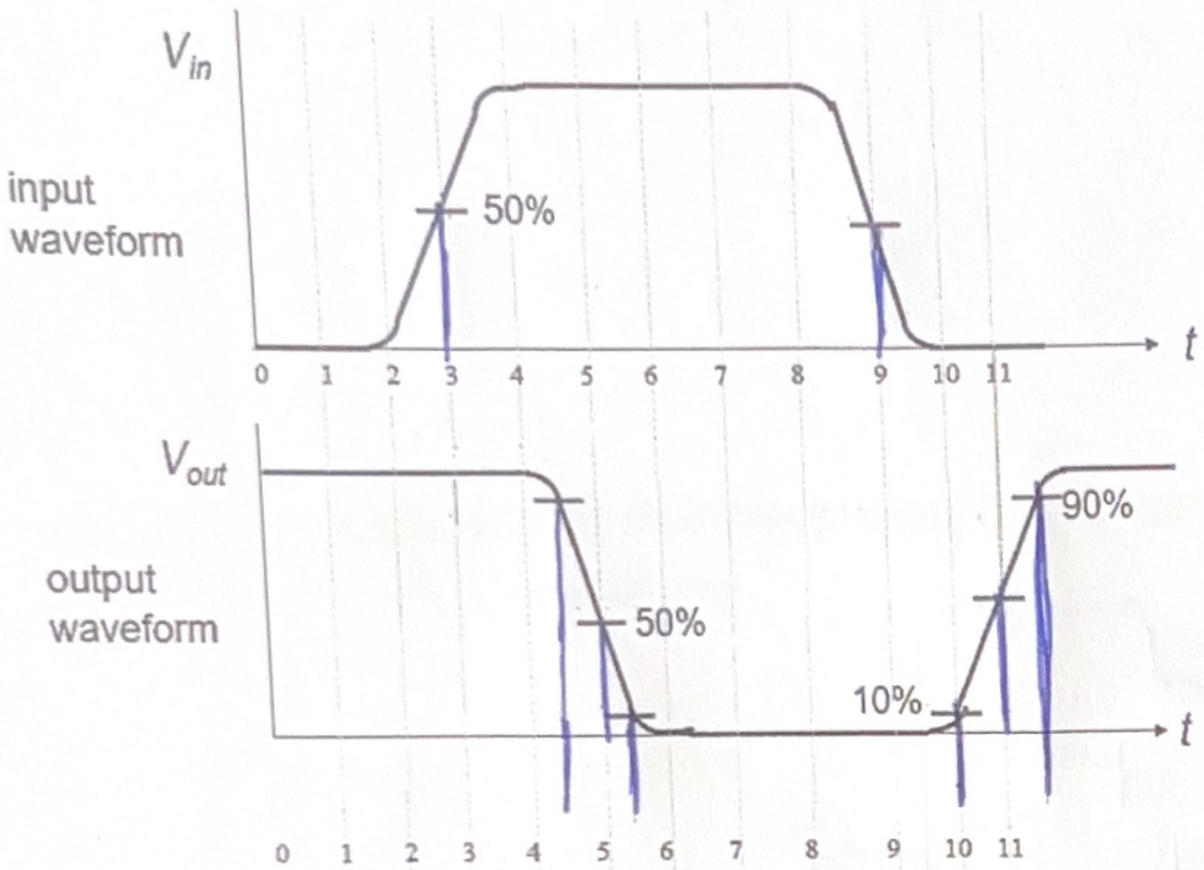
(a) Calculate the propagation delay (t_p) of the inverter (Hint: Calculate t_{pHL} and t_{pLH}); Show the steps

$t_{pLH} = 11 - 9 = 2$

$t_{pHL} = 5 - 3 = 2$

$t_p = \frac{2+2}{2} = 2$

(b) Calculate rise time and fall time



$t_R = 12 - 10 = 2$

$t_f = 5.5 - 4.5 = 1$

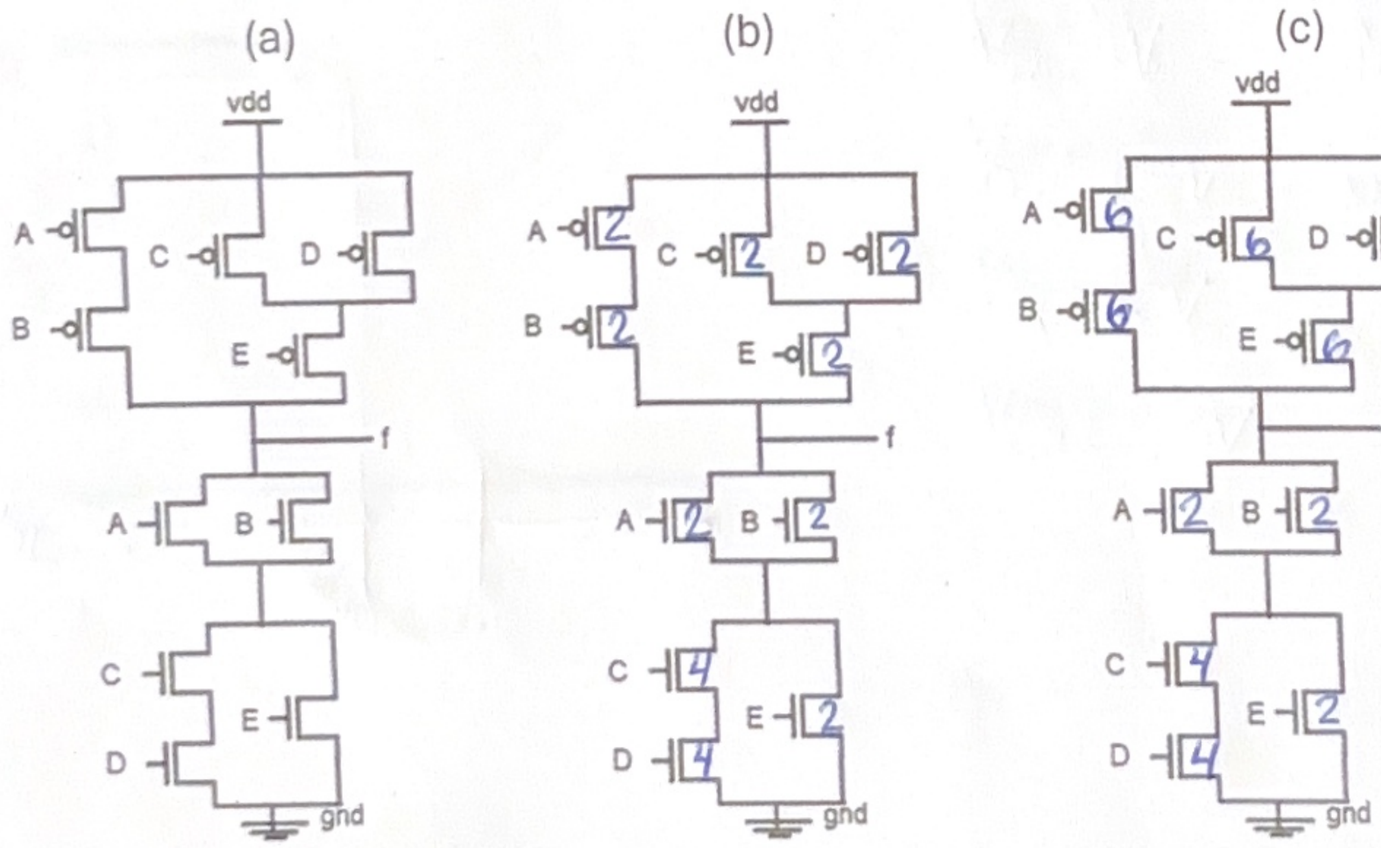
Fig. 2

5. [12 points]

(a) What is the logic function implemented by the static CMOS circuit shown in Fig 3(a)?

(b) Size the NMOS and PMOS devices for Performance (mark transistor size in Fig 3 (b)).

(c) Additionally, size the NMOS and PMOS devices for symmetric rise and fall times (mark transistor sizes in Fig 3 (c)).



$F = \overline{(A+B)(CD+E)}$

Fig. 3