CSE 493/593 FALL 2025 HOMEWORK 1

1. Given in Fig. 1 is the Voltage Transfer Characteristics of an inverter. Calculate the NM_L and NM_H.

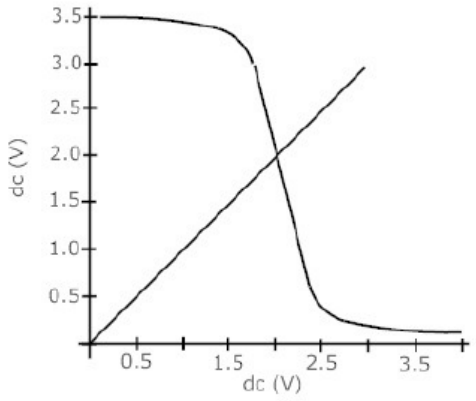

Fig. 1

2. Implement the given logic function using Complementary CMOS Logic.
   f = ^[((AB)+C)D]
3. Consider the following stick diagram. Draw the electrically equivalent transistor-level schematic. What logic equation does the circuit implement?

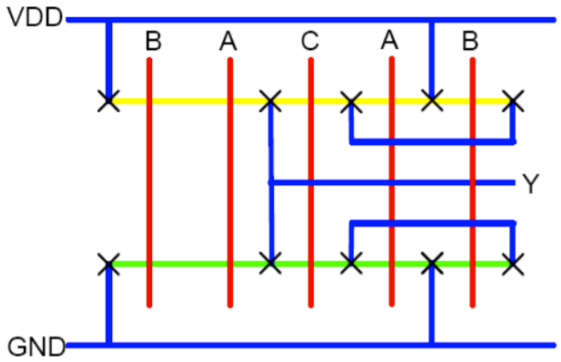

Fig. 2

4. Design a Half Adder (Sum and Carry) using Complementary CMOS Logic. [Hint: Derive logic expressions first]
5. Design a 4x1 multiplexer using Transmission Gate Logic.
   Considering inputs A, B, C, D; Select lines: S1, S2; Output: Out
6. The figure shows the input and output signals of a CMOS inverter. Calculate the following using the time instances mentioned in the figure.
   a. Fall time
   b. Rise time
   c. Propagation delay