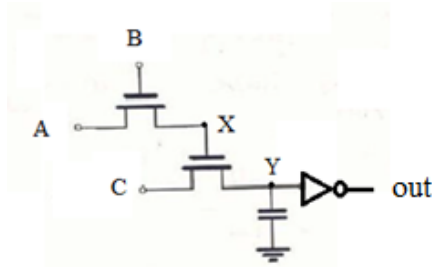
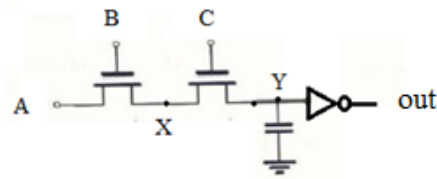


## CSE 493/593 Homework 2 Fall 2024

1. Determine the logic function implemented by
  - i.

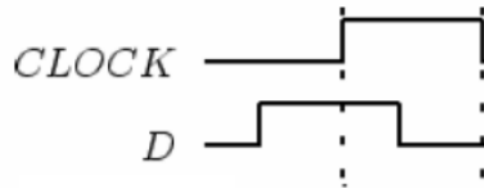


- ii.



2. Answer the following:

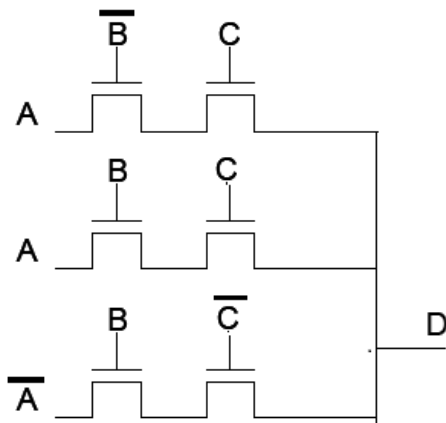
- i. What's difference in the function between a D latch and a D flip-flop?
- ii. Complete the timing diagrams for a positive-level-sensitive D latch and a positive-edge-triggered D flip-flop



Latch Q

Flipflop Q

3. Consider the circuit in Fig. below. What is the logic function implemented by this circuit?



## CSE 493/593 Homework 2 Fall 2024

4. How can you manipulate threshold voltage using body-biasing?
5. In order to drive a large capacitance ( $C_L = 20$  pF) from a minimum size gate (with input capacitance  $C_i = 10$  fF), you decide to introduce a three-staged buffer. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size.

(Hint: Sizing factor  $f = \sqrt[N]{C_L/C_{g,1}} = \sqrt[N]{F}$  ;

Minimum delay through the chain  $t_p = Nt_{p0}(1 + \sqrt[N]{F}/\gamma)$

- a. Determine the sizing of the three additional buffer stages that will minimize the propagation delay.
- b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? Consider  $\gamma=1$ .
6. Implement the given logic function using Complementary CMOS logic. (Transistor level diagram).  $F = \overline{((A+B)C+D)EF}$

Size all the transistors for

- a. Performance
- b. Symmetric rise and fall times