1. Consider the circuit in Fig. 1. Assume that all input combinations are equally likely. Let Cx=0.8fF, and CL=12fF.
   a. Calculate the activity factor for the output (F).
   b. Calculate the dynamic power consumption if the inputs are switching at rate of 200MHz at a supply voltage of 2.5V

   (Hint 1: If input probabilities are not given, consider them to be 0.5)

   (Hint 2: For total dynamic power consumption, calculate and add dynamic power consumption for all gates)

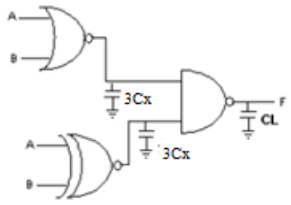

Fig. 1

2. For the circuit shown in Fig. 2, derive the transitional probability $P_{0\to1}$, given $P_A = 0.3$, $P_B = 0.5$, $P_C = 0.8$, $P_D = 0.4$. P_A, P_B, P_C and P_D indicate the probabilities that A, B, C and D are 1 respectively.

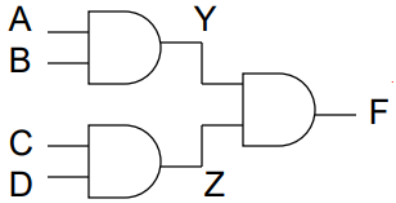

Fig. 2

3. Compute the switching probability of the output node F for both the chain and tree implementations of the circuit. P(A=1) = P(B=1) = P(C=1) = P(D=1) = 0.3. Which is better with regard to dynamic power?

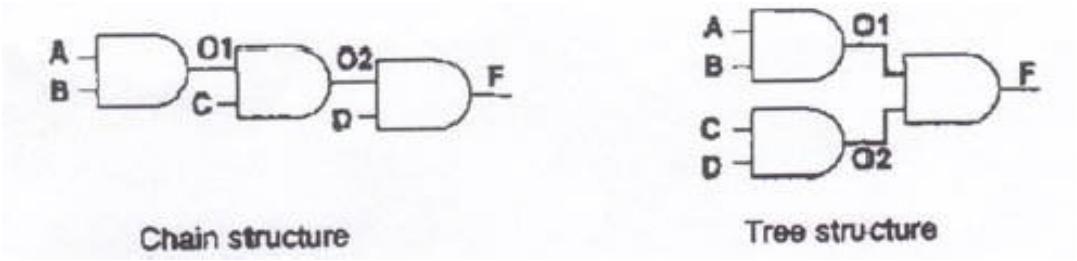

Fig. 3

4. Considering the logic circuit in Fig. 3, identify the critical path. Describe how you can achieve low power using
   a. Multi-V_{DD} technique
   b. Multi-V_T technique.

   Justify your answer.

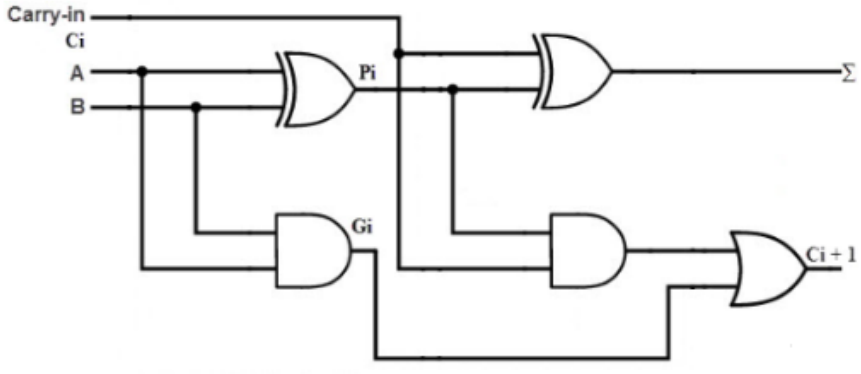

Fig. 4