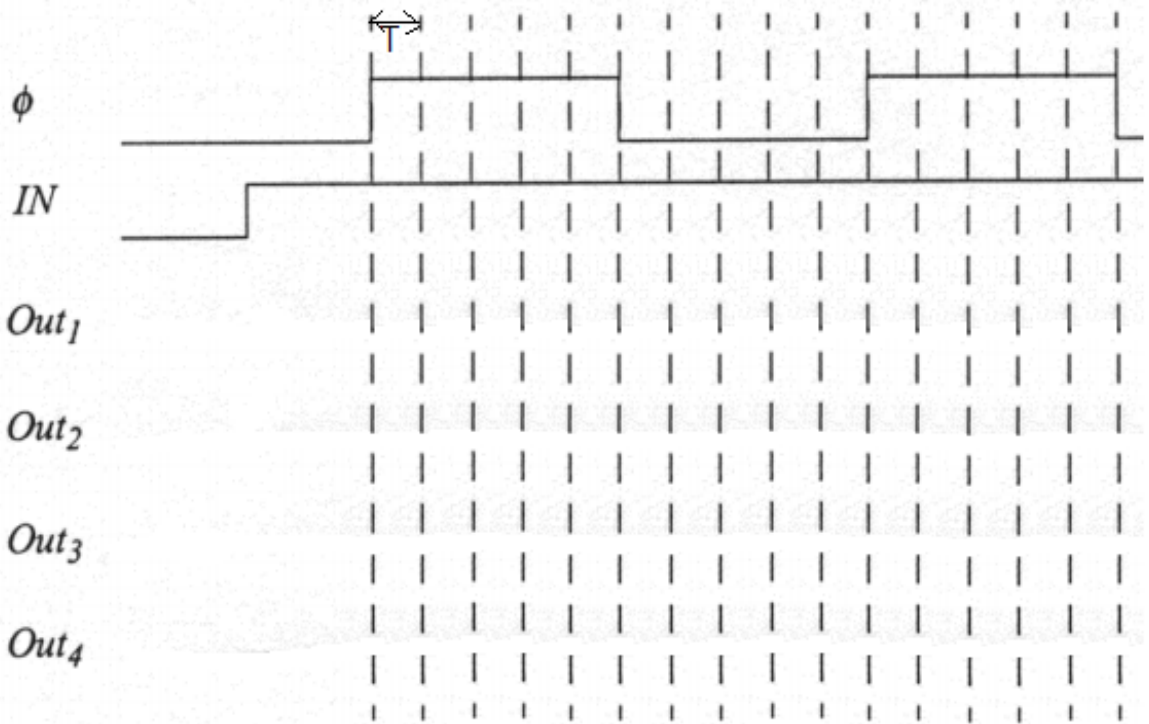
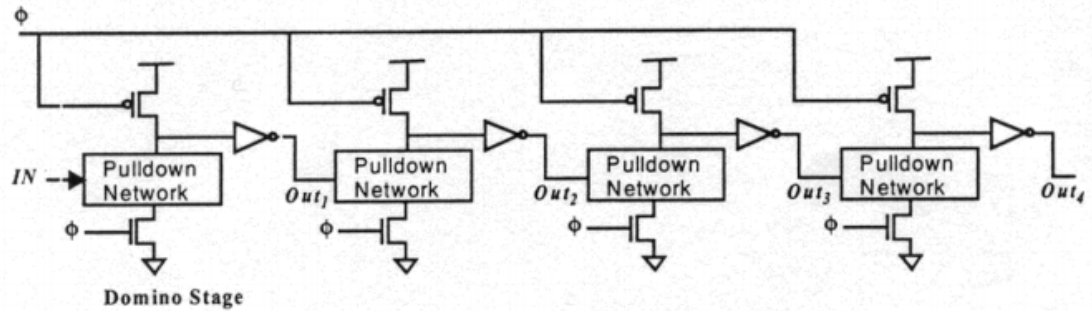


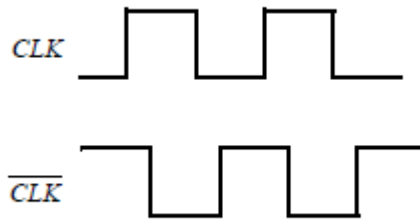
CSE 493/593 FALL 2025 – HOMEWORK 4

1. Consider the logic function $X = \neg((A(B+CD)E) + (FG(H+I)))$. Implement the function using Dynamic CMOS Logic.
2. Consider the 4-stage domino logic circuit as shown below. Assume that each of the PDN in the figure has a single NMOS transistor. Assume the precharge time, evaluate time, propagation delay of the static inverter are all equal to $T/2$ each (with T a time unit). Also assume zero rise and fall times for all signals. Complete the timing diagram for signals Out_1 , Out_2 , Out_3 and Out_4 if the IN signal goes high at the rising edge of the clock ϕ . Assume clock period is T .



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3. Describe how H-tree clock distribution scheme achieves the following:
 - a. Reduced clock skew
 - b. Reduced power consumption
4. How does clock skew differ from clock jitter?
5. From the clock waveform given below,



- a. identify regions of (1,1) overlap and (0,0) overlap.
- b. How can you overcome this issue?