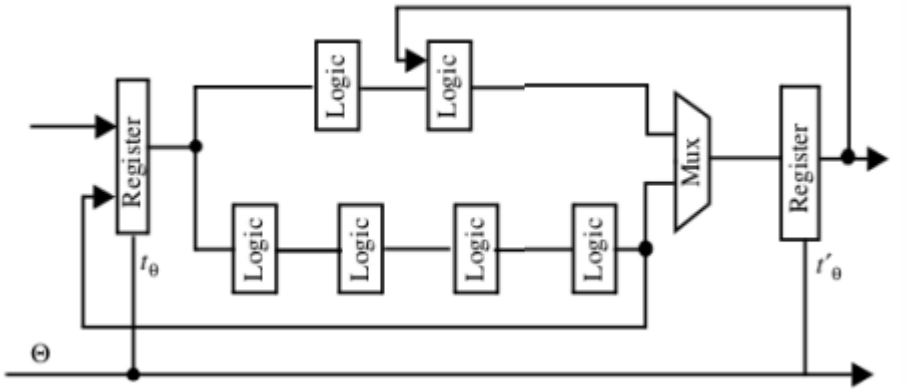
CSE 493/593 FALL 2024 HOMEWORK 5

1.
   a. Explain how Dynamic Frequency Scaling can achieve low power.
   b. Explain how Dynamic Voltage Scaling can achieve low power.

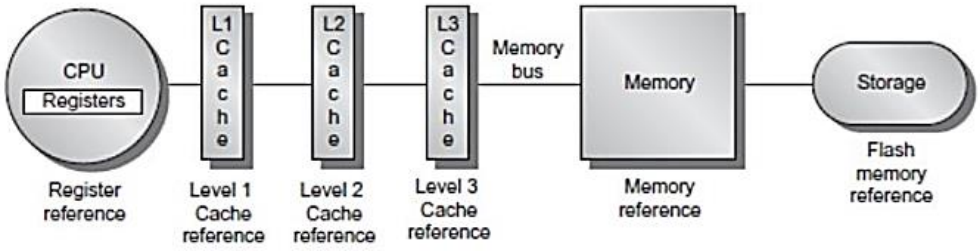
2. What is adaptive body biasing (ABB) technique? Describe how a designer can use this technique in low power design.

3. For the circuit shown below, assume a unit delay through the register, multiplexer and logic blocks. Assume that the registers, which are positive-edge triggered, have a unit setup time.



   Determine minimum clock period disregarding clock skew.
   (Hint: T ≥ tc-q + tlogic + tsu)

4. Given a typical memory hierarchy as shown below, list them in increasing order of
   a. Speed
   b. Cost per unit memory
   c. Size



5. Draw the schematic of 6T SRAM and explain its working.