CSE 490/590 Computer Architecture
Homework 1

Some of these problems are selected from our textbook examples.

1. Assume we have a computer where the clocks per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these are total 50% of the instructions. If the miss penalty of 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? (Answer: textbook C-5).

2. Determine the number of bits necessary for each of the cache address fields (i.e., tag, index, and block offset) for each of the following cache configurations. Assume that the address space is 32-bit.

   (a) Total cache size: 128KB, fully associative, byte-addressable memory (i.e., each memory address points to a byte, not a word), cache block size: 16 bytes
   (Answer: 28-bit tag, 0-bit index, and 4-bit offset)

   (b) Total cache size: 256KB, 4-way associative, word-addressable memory (i.e., each memory address points to a word, not a byte), cache block size: 8 words, word size: 4 bytes.
   (Answer: 18-bit tag, 11-bit index, and 3-bit offset)

   (c) Total cache size: 256KB, 2-way associative, byte-addressable memory, cache block size: 8 words, word size: 4 bytes.
   (Answer: 15-bit tag, 12-bit index, and 5-bit offset)

3. Assume fully associative write-back cache with many cache entries that starts empty. Below is a sequence of five memory operations (the address is in square brackets):

   ```
   Write Mem[100];
   Write Mem[100];
   Read Mem[200];
   Write Mem[200];
   Write Mem[100];
   ```

   What are the number of hits and misses when using no-write allocate versus write allocate? (Answer: textbook C-11)

4. Let's use an in-order execution computer. Assume the cache miss penalty is 200 clock cycles, and all instructions normally take 1.0 clock cycles (ignoring memory stalls). Assume the average miss rate is 2%, there is an average of 1.5 memory references per instruction, and the average number of cache misses per 1000 instructions is 30. What is the impact on performance when behavior of the cache is included? Calculate the impact using both misses per instruction and miss rate. (Answer: textbook C-17)

5. Figure C.11 (from the textbook) shows the actual miss rates plotted in Figure C.11 (from the textbook). Assume the memory system takes 80 clock cycles of overhead and then delivers 16 bytes every 2 clock cycles. Thus, it can supply 16 bytes in 82 clock cycles, 32 bytes in 84 clock cycles, and so on. Which block size has the smallest average memory access time for each cache size in Figure C.11? (Answer: textbook C-26).

6. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 emmory references per instruction. What is the average memory access time and average stall cycles per instruction? Ignore the impact of writes. (Answer: textbook C-31)