Last time…

- Dynamic address translation
  - Base and bound registers
  - Memory fragmentation problem
- Paged memory
  - Pages form an entire program
  - Uses page tables
- Demand paging
  - Hardware-assisted page swapping

Modern Virtual Memory Systems

- Illusion of a large, private, uniform store

Protection & Privacy

Several users, each with their private address space and one or more shared address spaces
page table = name space

Demand Paging

Provides the ability to run programs larger than the primary memory
Hides differences in machine configurations

The price is address translation on each memory reference

Size of Linear Page Table

With 32-bit addresses, 4-KB pages & 4-byte PTEs:

\[ \Rightarrow 2^{20} \text{ PTEs, i.e. 4 MB page table per user} \]
\[ \Rightarrow 4 \text{ GB of swap needed to back up full virtual address space} \]

Larger pages?

- Internal fragmentation (Not all memory in page is used)
- Larger page fault penalty (more time to read from disk)

What about 64-bit virtual address space???

- Even 1MB pages would require \(2^{44}\) 8-byte PTEs (35 TB!)

What is the “saving grace”? 

Linear Page Table

- Page Table Entry (PTE) contains:
  - A bit to indicate if a page exists
  - PPN (physical page number) for a memory-resident page
  - DPN (disk page number) for a page on the disk
  - Status bits for protection and usage
- OS sets the Page Table Base Register whenever active user process changes

Hierarchical Page Table

Virtual Address

\[
\begin{align*}
31 & 22 & 21 & 12 & 11 & 0 \\
\end{align*}
\]

Root of the Current Page Table

(Processor Register)

Level 1 Page Table

Level 2 Page Tables

Data Pages

Physical Memory

Page in primary memory
Page in secondary memory
PTE of a nonexistent page

What about the “saving grace”?
Address Translation & Protection

- Every instruction and data access needs address translation and protection checks
- A good VM design needs to be fast (~ one cycle) and space efficient

TLB Designs

- Typically 32-128 entries, usually fully associative
- Each entry maps a large page, hence less spatial locality across pages
- More likely that two entries conflict
- Larger systems sometimes have multi-level (L1 and L2) TLBs
- Random or FIFO replacement policy
- No process information in TLB?
- TLB Reach: Size of largest virtual address space that can be simultaneously mapped by TLB

Example: 64 TLB entries, 4KB pages, one page per entry

TLB Reach = 64 entries * 4 KB = 256 KB (if contiguous)

Handling a TLB Miss

Software (MIPS, Alpha)
- TLB miss causes an exception and the operating system walks the page tables and reloads TLB. A privileged "untranslated" addressing mode used for walk

Hardware (SPARC v8, x86, PowerPC)
- A memory management unit (MMU) walks the page tables and reloads the TLB
- If a missing (data or PT) page is encountered during the TLB reloading, MMU gives up and signals a Page-Fault exception for the original instruction

Translation Lookaside Buffers

Address translation is very expensive!
- In a two-level page table, each reference becomes several memory accesses

Solution: Cache translations in TLB
- TLB hit ⇒ Single Cycle Translation
- TLB miss ⇒ Page-Table Walk to refill
Hierarchical Page Table Walk: SPARC v8

Virtual Address

<table>
<thead>
<tr>
<th>Index 1</th>
<th>Index 2</th>
<th>Index 3</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>23</td>
<td>17</td>
<td>11</td>
</tr>
</tbody>
</table>

MMU does this table walk in hardware on a TLB miss

Address Translation: putting it all together

Address Translation in CPU Pipeline

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