Week 4

Announcement

Office Hours changed

Office hours :

-Monday 10-11

- Tuesday 11-12
- Friday 12-1

Behavioral Modeling --- Continue

Conditional Statements

- Syntax
 - if (*expression*) then clause

else

else clause

- Note:
 - Else clause is optional
- Conditional Operator
 - Can be used in place of If...Then...Else
 - Syntax: Condition ? True Expression : False Expression ;

- Case
 - Syntax
- case (expression)

```
alternative 1 : statement(s) 1 ;
alternative 2 : statement(s) 2 ;
```

```
•••
```

...

```
alternative n : statement(s) n ;
default : default statement(s) ;
```

```
endcase
```

- Default
 - Implemented when none of the alternatives are true
- Variations
 - Replace case with casex or casez for comparing don't cares or high impedance states

Operators

Operation Type	Symbol	Operation
Arithmetic	*	Multiplication
	/	Division
	+	Addition
	-	Subtraction
	%	Modulus
Logical	!	Negation
	&&	AND
	1	OR
Relational	>	Greater Than
	<	Less Than
	<=	Greater Than or Equal To
	>=	Less Than or Equal To
Equality	==	Equality
	!=	Inequality
	===	Case Equality
	!==	Case Inequality

Samir Palnitkar, Verilog HDL A Guide to Digital Design and Synthesis, Prentice Hall, Inc., 4[°] Edition, Table 6-1, pp. 92-93, 1996

Operators

Operation Type	Symbol	Operation
Bitwise	~	Bitwise Negation
Operation Type	&	Bitwise AND
		Bitwise OR
	^	Bitwise XOR
	~^ or ^~	Bitwise XNOR
Reduction	&	Reduction AND
	~&	Reduction NAND
	1	Reduction OR
	~	Reduction NOR
	^	Reduction XOR
	~^ or ^~	Reduction XNOR
Shift	>>	Right Shift
	<<	Left Shift
Concatenation	{ }	Concatentation
	{ { } } }	Replication
Conditional	?:	Conditional

Samir Palnitkar, Verilog HDL A Guide to Digital Design and Synthesis, Prentice Hall, Inc., 4" Edition, Table 6-1, pp. 92-93, 1996

Operator Precedence

Operators	Symbols	Precedence
Unary	+-!~	Highest
Multiply, Divide, Modulus	* / %	
Add, Subtract	+	
Shift	-	
Relational	%	
Equality	1	
Reduction	&,~&	
	^,~^	
	 , ∼	
Logical	&&	
	1	
Conditional	?:	Lowest

Samir Palnitkar, Verilog HDL A Guide to Digital Design and Synthesis, Prentice Hall, Inc., 4" Edition, Table 6-4, pp. 101-102, 1996

• Numbers

- Syntax
 - Sized
 - Size'Format Number
 - Size
 - » Number of digits
 - Format
 - » h (Hexadecimal)
 - » d (Decimal)
 - » o (Octal)
 - » b (Binary)
 - Number
 - » Number specified
 - Unsized
 - 'Format Number
 - Examples
 - 4'h a729
 - 'd 62923
 - 8'b 1101zzzz
 - 16'h x

Loops

• While

Syntax

while (*condition*)

begin

statement(s);

end

• For

Syntax

for (*initial condition; termination condition; control variable change*) begin

statement(s);

end

- Repeat
 - Repeats a given number of times based on the number, variable, or signal value given
 - Syntax

```
repeat (number, variable, or signal value)
begin
   statement(s);
end
```

Loops

- Forever
 - Statement executes forever
 - Can be disabled by the keyword disable
 - Syntax
 - forever statement;
 - Example
 - forever #10 clk=~clk;

- Concatenation Operator
 - {...,..}
 - Allows several wires to be combined together into a single multi-bit wire.

- In the next slides we will implement a full example to program the fpga.
- Try to follow these step to create your first project.

- Open the ISE project Navigator



- Type the project name

ISE	🔤 New Project Wizard 🛛 🔹 💽					
	Create New Project Specify project loc	ation and type.				
	Enter a name, locatio	ons, and comment for the project				
	N <u>a</u> me:	circuit				
	Location:	C:\Documents and Settings\circuit				
	Working Directory:	C:\Documents and Settings\circuit				
	Description:					
	Select the type of to	p-level source for the project				
	Top-level source typ	e:				
	Schematic					
	More Info					

- Select these options then click next

Property Name	Value	
Product Category	All	~
Family	Spartan3E	~
Device	XC35100E	~
Package	CP132	~
5peed	-4	~
Top-Level Source Type	Schematic	~
5ynthesis Tool	XST (VHDL/Verilog)	~
5imulator	ISim (VHDL/Verilog)	~
Preferred Language	Verilog	~
Property Specification in Project File	Store all values	~
Manual Compile Order		
VHDL Source Analysis Standard	VHDL-93	~

- click finish

🔤 New Project Wizard 🛛 🔀				
Project Summary Project Navigator will create a new project with the following specifications.				
Project: Project Name: circuit Project Path: C:\Documents and Settings\circuit Working Directory: C:\Documents and Settings\circuit Description: Top Level Source Type: Schematic				
Device: Device Family: Spartan3E Device: xc3s100e Package: cp132 Speed: -4				
Synthesis Tool: XST (VHDL/Verilog) Simulator: ISim (VHDL/Verilog) Preferred Language: Verilog Property Specification in Project File: Store all values Manual Compile Order: false VHDL Source Analysis Standard: VHDL-93				
Message Filtering: disabled More Info < Back				

- Select Project \rightarrow new source

155	ISE Proj	ect Na	vigator (M.81d) - C:\Documer	ments and Settings\blink_led\blink_led.xise	
Eile	e <u>E</u> dit	⊻iew	Project Source Process Tools	ools <u>W</u> indow La <u>v</u> out <u>H</u> elp	
.[) 🖻 🖥	101	Mew Source		
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	View: 🧿) (\$\$	Add Copy of Source		
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N F		from t using	Arc <u>h</u> ive Generate <u>T</u> cl Script		
		Librar	Design <u>G</u> oals & Strategies		
		Use:	Design Summary/ <u>R</u> eports		
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	Console		Errors 🔝 Warnings 🕅 🕅 Find	Find in Files Results	
Add	a new soi	urce to	the project		

- Select Verilog module and write the file name, then click next

🔤 New Source Wizard 📉 🔀			
Select Source Type Select source type, file name and its location.			
 IP (CORE Generator & Architecture Wizard) Schematic User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Library VHDL Package VHDL Test Bench Embedded Processor 	Eile name: circuit Logation: C:\Documents and Settings\circuit		
More Info			

- click next

🔤 New Source Wizard 🛛 🔹 🔀						×	
Define Module Specify ports for module.							
Module name	circuit						
	Port Name	Direction		Bus	MSB	LSB	
		input	~				
		input	~				
		input	~				
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More Info]		< <u>B</u> a	ack	<u>N</u> ext >	Cance	el

- Click Finish

🚾 New Source Wizard	×
Summary Project Navigator will create a new skeleton source with the following specifications.	
Add to Project: Yes Source Directory: C:\Documents and Settings\circuit Source Type: Verilog Module Source Name: circuit.v Module name: circuit Port Definitions:	
More Info	

- The file will be created and it will look like as below



- Add your code shown

🖥 ISE Project Navigator (M. 81d) - C:\Documents and Settings\circuit\circuit.xise - [circuit.v*]				
Eile Edit View Project Source Process	Tools <u>W</u> indow La <u>v</u> out <u>H</u> elp	_ @ X		
i 🗋 🎓 🖬 🕼 😓 i 🕺 🖬 🔂 💌 i	× » 🔑 🔎 😥 🎮 🔄 🦂 🔚 🖽 🖻 🖉 🖓 👔 🕨 🔤 🛠 👂			
Design ↔ □ ₽ × View:	<pre>1 'timescale ins / 1ps 2 ////////////////////////////////////</pre>			
Image: Second state sta	<pre>21 module circuit(switch, enable, led); 22 input switch; 23 input enable; 24 output led; 25 integer count; 26 reg led; 27 28 always@(switch) 29 begin 30 if (enable==1) 31 begin 32 led=switch; 33 end 34 else 35 begin 36 led=0; 37 end 38 end 39 40 endmodule 41</pre>			
Start 📴 Design 🚺 Files 🖺 Libraries	circuit.v* 🛛 🗴 Design Summary	>		
		Ln 36 Col 10 Verilog		

- You can copy the code from here and paste it in your project

module circuit(switch, enable, led); input switch; input enable; output led; integer count; reg led;

> always @(switch) begin if (enable==1) begin led=switch; end else begin led=0; end end

endmodule

- To simulate the project select new source



- Select Verilog Test Fixture and write the file name then click next

🔤 New Source Wizard 🛛 🛛 🔀				
Select Source Type Select source type, file name and its location.				
BMM File ChipScope Definition and Connection File Implementation Constraints File IP (CORE Generator & Architecture Wizard) MEM File Schematic User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Library VHDL Test Bench Embedded Processor	Eile name: test1 Logation: C:\Documents and Settings\circuit			
More Info	Next > Cancel			

- Select the circuit module then click next



- click Finish to create the test file

🔤 New Source Wizard 🛛 💽
Summary Project Navigator will create a new skeleton source with the following specifications.
Add to Project: Yes Source Directory: C:\Documents and Settings\circuit Source Type: Verilog Test Fixture Source Name: test1.v Association: circuit
More Info

- This is how it will look like



- Add your simulation code to the test file

	SE Project Navigator (M.81d) - C:\Docum	ents a	and Setti	gs\circuit\circuit.xise - [test1.v]	
E F	ile Edit View Project Source Process	Tools	Window	Layout Help	- 8 ×
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Desig	n ↔□₽×	•	31	// Outputs	~
T	View: 💿 🉀 Implementation 🔿 🔜 Simulation	ME	32	wire led;	
E	Hierarchy		33		
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엽티	🖨 🔲 xc3s100e-4cp132	5	35	suitch (suitch)	
	- V 🛱 circuit (circuit.v)	-	37	.emble(enable).	
400.000		10	38	.led(led)	
9		<u> </u>	39) :	
671		1	40		
aut.		94	41	initial begin	
1		574	42	// Initialize Inputs	
			43	switch = 0;	
		*	44	enable = 0;	
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			46	// wait 100 hs 10f global feset to linish	
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			51	#100;	
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			53	enable = 1;	
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~44			60	switch = 1;	
			61	enable = 0;	
			62		
			63	#100;	
			64	switch = 0;	
			65	enable = 0;	
			66	4100	
			67	#IUU; evitab = 1.	
			69	enable = 1:	
			70	// Add stimulus here	
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			72	end	
			73		~
			<	· · ·	>
150	Start 💷 Design 🖺 Files 🖺 Libraries	E	and a second	circuit.v* 🗵 🗵 Design Summary 🖾 📄 test1.v 🖾	- Annala -
					Ln 55 Col 12 Verilog
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- Select the simulation option from Design tab

155	SE Project Navigator (M.81d) - C:\Docum	ients	and Sett	igs\circuit\circuit.xise - [test1.v]		
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1		2	42	// Initialize Inputs		
-		24	43	switch = 0;		
		**	44	enable = 0;		
			45			
			46	// Wait 100 ns for global reset to finish		
		1	47	#100;		
			48	switch = 0;		
			49	enable = 1;		
			50	#100.		
			51	#100; switch = 1:		
			52	switch = 1;		
-			53			
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即打	No single design module is selected.		56	switch = 0;		
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			63	#100;		
			64	switch = 0;		
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			68	Switch = 1;		
			- 69 - 70	<pre>chapic = 1; // Add stimulus here</pre>		
			70	// Add Soludids Hele		
			72	end		
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					Ln 55 Col 12 Verilog	

- Select test1.v file and D-Click Simulate Behavioral Model to open ISIM simulator

151	ISE Project Navigator (M. 81d) - C:\Docum	ents d	and Setti	ngs\circuit\circuit.xise - [test1.v]			
B	<u>File Edit View Project Source Process</u>	iew P <u>r</u> oject <u>S</u> ource <u>P</u> rocess <u>T</u> ools <u>W</u> indow La <u>v</u> out <u>H</u> elp					
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5		1	38	. Led (led)			
		A	39	10			
623		-	41	initial begin			
		10	42	// Initialize Inputs			
-		24	43	switch = 0;			
-		X	44	enable = 0;			
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			48	switch = 0;			
			49	enable = 1;			
			50	****			
			51				
			52	switch = 1;			
			53				
	C2 No Processes Running		55	#100:			
P'r	Processes: test1		56	switch = 0;			
ENH:	😑 😼 ISim Simulator		57	enable = 1;			
×4	- N Behavioral Check Syntax		58				
9£	Simulate Behavioral Model		59	#100;			
_			60	switch = 1;			
			61	enable = 0;			
			62				
			63	#100;			
			64	switch = 0;			
			65	enable = U;			
			66	4100.			
			20	witch = 1.			
			69	enable = 1:			
			70	// Add stimulus here			
			71				
			72	end			
			73		~		
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ISE	Start 📴 Design 🚺 Files 🚺 Libraries	E		circuit.v* 🛛 🗵 Design Summary 🛛 🖹 test1 v 🥅	LOUI.		
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					En 55 Col 12 Verilog		

- ISIM application, use zoom in, out to view the results

🔜 ISim (M. 81 d) - [Default.wcfg]								
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ISim M.81d (signature 0xcb73ee62)								
This is a Full version of ISim.								
Simulator is doing circuit initialization process.								
Finished circuit initialization process.								
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Console 🔍 🖲 Breakpoints 🕅 🏧 Fin	d in Files Results 🛛 📷	Search Results						
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- To implement the code on the fpga board go to implementation mode

199	SE Project Navigator (M.81d) - C:\Docum	ents a	und Settin	igs\circuit\circuit.xise - [test1.v]				
	<u>File E</u> dit <u>V</u> iew P <u>r</u> oject <u>S</u> ource <u>P</u> rocess	Tools	jools <u>W</u> indow La <u>y</u> out <u>H</u> elp _ = = ×					
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E	Hierarchy		33	// There are a few that the second and a structure				
Ch	- 🧧 circuit	=	34	circuit wut (
a	😑 🗍 xc3s100e-4cp132	-	36	.switch(switch).				
00	🛶 💟 🚛 circuit (circuit,v)	12	37	.enable(enable),				
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			39					
12		1	40					
		36	41	initial begin				
		54	42	// Initialize Inputs				
		0	43	switch = 0;				
		24	44	enable = 0;				
			45	// Noit 100 we faw glabal waast to finish				
			40	// Wait 100 hs for grobal reset to rinish #100.				
			48	switch = 0;				
			49	enable = 1;				
			50					
			51	#100;				
			52	switch = 1;				
		5	53	enable = 1;				
	🌏 No Processes Running		54					
Enter	Levi .	ř.	55	#100;				
14	Processes: circuit		56	switch = U;				
聖	Design Summary/Reports		57	enable = 1;				
De	Pri + V User Constraints		50	#100.				
14	Synthesize - XST		60	switch = 1;				
			61	enable = 0;				
	Generate Programming File		62					
	🕀 🐝 Configure Target Device		63	#100;				
	Analyze Design Using ChipScope		64	switch = 0;				
			65	enable = 0;				
			66					
			67	#100;				
			68	switch = 1;				
			69	enaple = 1;				
			70	// Add Stimulds here				
			72	end				
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-	Design III Files II Libraries			uruut.v 🔄 🚈 Design Summary (out or date) 🔛 📋 test1.v 🔛				
					Ln 53 Col 14 Verilog			

- Select circuit.v file and select I/O planning (PlanAhead-Presynthesis) to open PlanAhead application to assign the fpga I/O ports to the code I/O



- Click yes to create UCF file and open Planahead application



- Planahead Application after its opened



-Select I/O ports, drag and drop each of them to Pin in the Package figure, refer to <u>http://www.digilentinc.com/Data/Products/BASYS2/Basys2 rm.pdf</u> to find the pin definition



- After pin assignment



- Click save design and exit



- To Prepare the .bit File to Program the FPGA,

- Set the FPGA Startup Clock to JTAG Clock, Right click on Generate

Programming File in the Processes Window, select Process Properties



Change Startup Options to JTAG clock as shown, then press OK

Process Properties - Startup Op	tions			×
<u>C</u> ategory	Switch Name	Property Name	Value	
General Options Configuration Options	-g StartUpClk:	FPGA Start-Up Clock	JTAG Clock	
	-g DONE_cycle:	Done (Output Events)	Default (4)	-
	-g GTS_cycle:	Enable Outputs (Output Events)	Default (5)	-
	-g GWE_cycle:	Release Write Enable (Output Events)	Default (6)	-
	-g LCK_cycle:	Wait for DLL Lock (Output Events)	Default (NoWait)	-
	-g DriveDone:	Drive Done Pin High		
	Pr	operty display level: Standard 🔽 🖸	Display <u>s</u> witch names Default	
		OK Can	cel <u>A</u> pply Help].

Create the .bit file, Double click on Generate Programming File in the Processes Window

🔤 ISE Project Navigator (M.81d) - C:\Docun	nents and S	tings\circuit\circuit.xise - [test1.v]				
Eile Edit View Project Source Process	ocess Iools Window Layout Help 🗧 🗗 🗙					
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View: 💿 🎒 Implementation 🔿 🎆 Simulation	N 33	wire led;				
E Hierarchy	3					
	3	// Instantiate the Unit Under Test (UUT)				
□ → □ xc3s100e-4cp132	3.	circuit uut (
🖳 🕀 🕅 👫 circuit (circuit.v)	3	.switch(switch),				
		led(led)				
£	3	1:				
679	1 4	<u>976</u>				
	96 4	initial begin				
	4	// Initialize Inputs				
	7 4:	switch = 0;				
	> 4	enable = 0;				
	4/					
	4	// Wait 100 ns for global reset to finish				
	4	#100;				
	4	switch = 0; enable = 1.				
	5	chart i,				
	5	#100:				
	5	switch = 1;				
	5	enable = 1;				
No Processes Running	5					
	5	#100;				
Processes: circuit	5	switch = 0;				
👷 🗁 🚬 Design Summary/Reports	5'	enable = 1;				
🕀 🎽 Design Utilities	51	#100				
🕅 🗟 🎬 User Constraints	59	#100; 				
Create Timing Constraints	6	Switch - 1;				
I/O Pin Planning (PlanAnead) - P	6					
Floorplan Area (IO/Logic (PlanAb	6	#100;				
Synthesize - XST	6	switch = 0;				
🗄 🔁 Implement Design	6	enable = 0;				
Generate Programming File	6					
🕀 🛞 Configure Target Device	6'	#100;				
Analyze Design Using ChipScope	6/	switch = 1;				
	65	enable = 1;				
	70	// Add stimulus here				
		and				
	7					
	-		×			
			2			
Start Design Files Dibraries		circuit.v 🔟 🖉 Design Summary (out of date) 🔛 📋 test1.v 🗵				
			Ln 54 Col 7 Verilog			

Make sure that every thing is compiling and building

🔤 ISE Project Navigator (M. 81 d) - C:\Docume	ents a	und Settin	gs\circuit\circuit.xise - [test1.v]	
Elle Edit View Project Source Process Iools Window Layout Help				_ 8 ×
S 🖬 🗶 🛛 🖧 🛛 😓 📲 😓 🔁	i >) i 🏓 🏓	8 8 × 8 × 1 = = = = × 8 × 1 × 2 × 1 8	
Design ↔ □ 큠 ×	1	31	// Outputs	~
📑 View: 💿 🎒 Implementation 🔿 🚂 Simulation	NE.	32	wire led;	
Fill Hierarchy	-	33		
		34	// Instantiate the Unit Under Test (UUT)	
□ □ □ xc3s100e-4cn132	5	35	circuit uut (
		36	.switch(switch),	
		37	.enable(enable),	
	兰	38	. Ted (Ted)	
	A	40		
E23		41	initial begin	
	~	42	// Initialize Inputs	
	2	43	switch = 0;	
	*	44	enable = 0;	
		45		
		46	// Wait 100 ns for global reset to finish	
		47	#100;	
		48	switch = 0;	
		49	enable = 1;	
		50		
		51	#100;	
		52	switch = 1;	
		53	enable - I;	
No Processes Running		54	#100.	
Processes: circuit		56	switch = 0:	
Design Summary/Reports		57	enable = 1;	
Design Utilities		58		
🖳 🔄 🈼 User Constraints		59	#100;	
Create Timing Constraints		60	switch = 1;	
I/O Pin Planning (PlanAhead) - P		61	enable = 0;	
I/O Pin Planning (PlanAhead) - P		62		
Floorplan Area/IO/Logic (PlanAh		63	#100;	
🕀 🔃 🖉 Synthesize - XST		64	switch = 0;	
🖨 🍋 🦉 Implement Design		65	enable = 0;	
🕀 😳 Translate		66	#100-	
		67		
		60	amable = 1.	
Configure Target Deutice		70	// Add stimulus here	
Apalyze Design Lising ChinScope		71		
Hindiyze besign bing empscope		72	end	
		73		
				×
	EN			
Design Hies I Libraries		cir	uu.v 🔤 🖉 Design Summary (Programming File Generated) 🔛 📋 test1.v 🔯	
				Ln 70 Col 22 Verilog

Connect Basys2 to your computer and make sure its correctly configured



Open Adept2.1 (Downloaded from Digilent's Website) <u>http://www.digilentinc.com/Products/Detail.cfm?NavPath=</u> <u>2,66,69&Prod=ADEPT</u>

A Digilent Adept	
BASYS2	Connect: Basys2 Product: Basys2 - 100 VO Ex Settings
	IT I Detailigs
FPGA XC3S100E	Browse Program
	Browse Program
Toitialize	Chain
Board information loaded. Found device ID: (5045093	<u>^</u>
Found device ID: 11c10093 Initialization Complete.	
Device 1: XC3S100E Device 2: XCF02S	
	<u> </u>

Click on Browse (next to FPGA Option) an select the bit file from the project Directory



▲ Digilent Adept	
BASYS 2	Connect: Basys2 Product: Basys2 - 100
Config Test Register I/O File I/	D I/O Ex Settings
FPGA XC3S100E circuit.bit	Browse Program
PROM XCF02S	Browse Program
Initia	ize Chain
Board information loaded. Found device ID: f5045093 Found device ID: 11c10093	
Initialization Complete. Device 1: XC3S100E Device 2: XCF02S	

Make sure the basys2 is on, click on the program, and test your fpga

🛆 Digilent Adept
BASYS2 [™] Connect: Basys2 V Product: Basys2 - 100
Config Test Register I/O File I/O I/O Ex Settings
FPGA XC3S100E circuit.bit Browse Program
PROM XCF02S Browse Program
Initialize Chain
Device 2: XCF02S Set Config file for XC3S100E: "C:\Documents and Settings\circuit\circuit.bit"
Preparing to program XC35100E Programming Verifying programming of device
Programming Successful.

Another example

 The following circuit will blink LED #0 when enabled Period = 2 seconds Enable = Switch #0 When Switch #0 is off, 	module blinking_led(clk, led, enable); input clk; output led; input enable; reg led; integer count;
LED #0 is off	always @(posedge clk)
	begin
	if (enable==0)
	begin
	count=0;
	led=0;
Pin Assignments	end
	else
	begin
•Clk	if (count > 5000000)
- B8	begin
• Enable (S) ((0)	count=0;
•Enable (SWO)	. led=~led;
- P11	end
•LED (LDO)	count = count+1;
- M5	end
	ena an des a duda
	enamoaule

Basys Board Resources

Basys board documentation and resources can be found at the Digilent Website. Click on <u>http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,790&Prod=BAS</u> <u>YS2</u> to go right to these resources.

Quick Links

<u>Reference Manual</u> http://www.digilentinc.com/Data/Products/BASYS2/Basys2_rm.pdf <u>Schematics</u> http://www.digilentinc.com/Data/Products/BASYS2/Basys2_sch.pdf

Adept Programming Suite

The Adept Programming Suite is required to the Basys2 board using the USB cable. It can be downloaded by clicking <u>http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,66,69&Prod=ADEPT</u>

Required Software

- Xilinx ISE WebPack
 - Project Navigator (Main workspace for verilog)
 - ISIM (Simulator)PlanAhead (to assign Pins)
- iVerliog (Simulator)
- Diligent
 - configuration and print the implementation of the fpga board

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